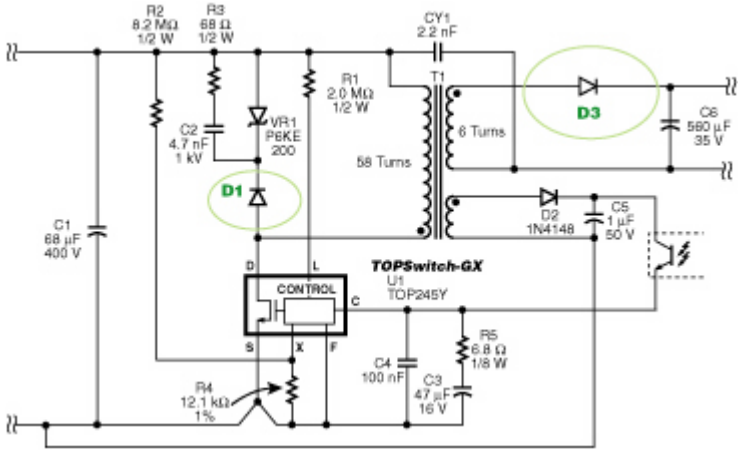
Puzzler 1

The schematic below shows a Flyback power supply built with a TOPSwitch® -GX power conversion IC. The following questions concern the selection of the output diode (D3) and the clamp diode (D1).

Question 1

Beginner Level



Input: 90-375 VDC

Output: 12 V, 2.5 A

Which diode or diodes from the following list are suitable for use as D3 and why?

1. 80 V, 5 A, Schottky (e.g. SB580)
2. 600 V, 3 A, Ultrafast (e.g. UF5406)
3. 50 V, 3 A, Rectifier (e.g. 1N5400)
4. 100 V, 8 A, Ultrafast (e.g. BYV29-100)
5. 45 V, 7.5 A, Schottky (e.g. MBR745)
6. 1000 V, 2.5 A, Fast (e.g. FR257)

Show the Answer

Answer 1

Answer is a and d

Diode	Diode Parameters	Suitability of Diode Parameters		
		Peak Reverse Voltage (V_{RRM})	Average Forward Current (I_{AVE})	Reverse Recovery Time (t_{rr})
(a) SB580	**80 V, 5 A**	**X**	**X***	**X**
(b) UF5406	600 V, 3 A, 75 ns	X	-	-
(c) 1N5400	50 V, 3 A, 2000 ns	-	-	-
(d) BYV29-100	**100 V, 8 A, 25 ns**	**X**	**X**	**X**
(e) MBR745	45 V, 7.5 A	-	X	X
(f) FR257	1000 V, 2.5 A, 500 ns	X	-	-

* With bench verification of temperature rise

Why?:

In selecting the output rectifier three key parameters should be considered; voltage rating, current rating and reverse recovery time.

Considering each of these in turn we can see which of the diodes is suitable.

Maximum repetitive reverse voltage (V_{RRM})

Ideally the diode selected should have a V_{RRM} rating $1.25 \cdot V_R$, where V_R is the reverse voltage seen by the diode. The 1.25 de-rating factor provides margin to take account of leakage inductance generated voltage spikes, and AC line transients that increase the DC bulk voltage temporarily plus reducing the device stress improves reliability.
Normally where people get into trouble is determining the value of V_R. You'd be forgiven for thinking that the reverse voltage seen by the diode is just the output voltage, here 12 V so anything above a 15 V diode would be fine. However the anode of D3 is connected to a Flyback transformer. This means that when the MOSFET inside U1 turns on, under maximum input line of 375 VDC ($265 \cdot VAC \times \sqrt{2}$) is seen across the primary. This voltage is transformed by the primary to secondary turns ratio and due to the phase of the windings drives the anode of the output diode negative. In this design the value of V_R is given by:

$V_R = V_O + (V_{MAX}) \cdot (N_S/N_P)$
$= 12 + 375 \cdot 6/58$
$= 50.7$ V

Applying the 1.25 V de-rating this gives a minimum diode rating of 63 V. The closest standard diode rating would be an 80 V Schottky or a 100 V PN diode.
Therefore all the diodes have an acceptable V RRM rating except (c) and (e).

Forward Current Rating (I_{AVE})

Diodes manufacturers generally specify the current rating as the average current through the diode or for a Flyback power supply the load current. In this design the specified output current is 2.5 A so a diode with a current rating above 2.5 A is acceptable right? Yes and no.

- The diode manufacturers provide de-rating curves so for example at a lead temperature of 100 °C a 3 A PN diode is actually a 1.5 A diode!
- Diode type. The choice between PN and Schottky and the actual voltage rating changes a diode's forward voltage. The lower the forward voltage drop, the lower the dissipation is for a given forward current.
- Overload fault conditions. All power supplies have some degree of overload capability. Due to tolerances a typical supply will be able to deliver significantly more than the specified output power, especially at high line. Therefore if an overload condition can exist then the diode should be sized to operate without overheating and failing. Products from Power Integrations significantly help here as the key parameters associated with power delivery (frequency and current limit) are very tightly specified, reducing the overload power. In addition line voltage power limiting is easy to add to reduce overload power. In this example the addition of R2 reduced the primary current limit as the line voltage increases and provides a very flat overload power characteristic with line voltage as shown below.

As a general rule of thumb select the current rating such that $I_{AVE} = 3 \times I_O$ irrespective if the diode is a PN or a Schottky type (although a Schottky diode will have lower dissipation check the maximum operating temperature – some are 25-50 ° C lower than a PN diode). Finally measure the diode temperature under maximum overload power, highest ambient to check it is within either internal or manufacturers design limits.
Looking at the diodes in the list to determine if they are acceptable or not:

Diode	**Rated I_{AVE}**	**Acceptable?**	**Notes**
(a) SB580	5 A	Yes - based on bench verification	I_{AVE} is only 2 x I_O it's a Schottky diode has a maximum temperature specification of 150 C and used in a supply with power limiting (R2 and R4 in schematic) so it's likely this diode would be acceptable.
(b) UF5406	3 A	No	I_{AVE} is only 1 or 1.2 x I_O - diodes would overheat
(c) 1N5400	3 A	No	
(f) FR257	2.5 A	No	
(d)BYV29-100	8 A	Yes	I_{AVE} is ≥3 x I_O and in a TO220 package. When attached to a suitable heatsink this diode is a good choice.

So diodes (a), (d) and (e) have an acceptable current rating but if you ruled out (a) that would also be ok.

Reverse recovery time (t_{rr})

An ideal diode would instantly block reverse current flow when a reverse bias is applied. In practice a Schottky approaches zero recovery time however for a PN diode it takes a finite time for charge stored in the diode to be swept away before it can block. The amount of charge is proportional to the current flowing through the diode.

This is significant as even a Flyback converter operating in discontinuous conduction mode will actually operate in continuous conduction mode at start-up meaning the output diode has to reverse recover with a significant forward current flowing. In this design the converter operates in continuous conduction mode some the diode has to recover with forward current on every switching cycle.

To prevent large reverse currents from flowing through the diode when the MOSFET in U1 turns on, applying a reverse voltage, the diode should have a reverse recovery time less than switching time. This means a recovery time of 50 ns or better.

Longer duration than this causes large primary side current spikes at the turn on event and high diode dissipation – for example the 1N5400 became hot enough to melt the solder holding into the PCB while taking the measurements for question 2.

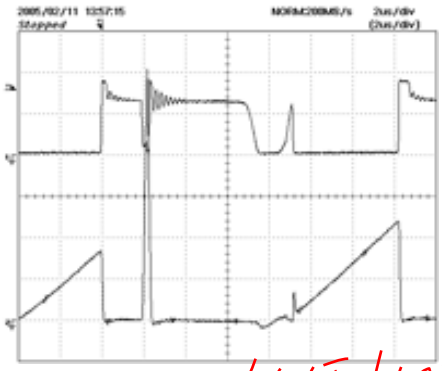
Diode	t_{rr}	Acceptable?	Notes
(a) SB580	0	Yes	
(b) UF5406	75 ns	No	
(c) 1N5400	-	No	Not specified but >>2000 ns
(f) FR257	500 ns	No	
(d) BYV29-100	25 ns	Yes	
(e) MBR745	0	Yes	

So diodes (a), (d) and (e) have an acceptable reverse recovery time.

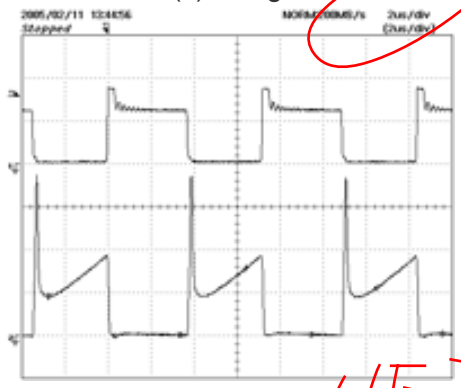
Question 2

Advanced Level

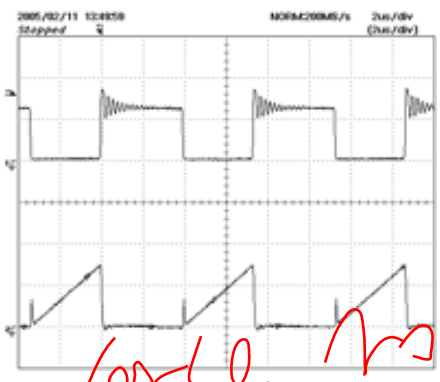
Below is a series of oscillograms showing the drain voltage (V_{DS}) and current (I_D) of U1, measured with the different diodes listed in question 1*. Can you match the resultant waveforms to the diode(s) that generated them?



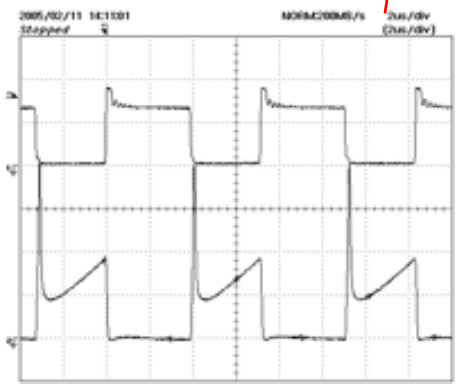
Waveform 1: 1N5400



Waveform 2: UF5406



Waveform 3: _____



Waveform 4: _____

*Test Conditions: 1.5 A load @ 115 V AC; Upper Trace V_{DS}=100 V/div; Lower Trace I_D=0.4 A/div, 2 µs/div

Show the Answer

Answer 2

Waveform	Associated Diode
1	(C) 1N5400
2	(B) UF5406s
3	(A) SB580, (D) BYV29-100 and (E) MBR745
4	(F) FR257

Why?:

As discussed for question 1, as the reverse recovery time of the diode increases so does the magnitude of the reverse current. This current is transformed according to the turns ratio of the transformer and results in a large drain current spike when the *TOPSwitch* turn on. Accordingly the slowest diode, the 1N5400 causes the largest spike – large enough to trigger the internal *TOPSwitch* current limit at the end of the 220 ns leading edge blanking time.

This waveform also shows the effect of the diode forward current on reverse recovery time. The next switching cycle occurs normally with almost no current spike, as there is no current flowing in the diode when it is reverse biased. As no energy was stored in the transformer due to the early termination of the switching cycle all the energy in the transformer is transferred to the load and the diode current falls to zero.

Next is sequence is the FR257, and the UF5406 both which have unacceptably high reverse currents. With a turns ratio of 58:6 the FR257 allowed a reverse current of 15.4 A (1.6 x 58/6) to flow during reverse recovery. This explains why this and all the slow diodes would have been destroyed had the test been longer than a few seconds.

The 25 ns reverse recovery of the BYV29-100 diode produces identical results to the Schottky – the spike now seen is purely due to parasitic capacitance, largely the capacitance of the primary winding.

Question 3

Expert Level

Diode	P_{IN} (W)	P_{OUT} (W)	η (%)
UF4005	36.18	30.23	83.6
1N4937	36.07	30.23	83.8
1N4007GP*	35.92	30.23	84.2
*Glass Passivated			

Selecting diodes with different recovery times for the clamp diode D1 has an interesting effect. The table shows the measured input power and resultant efficiency for the different diode tested. Can you explain the changes in efficiency and why the rectifier diode must be glass-passivated?

Show the Answer

Answer 3

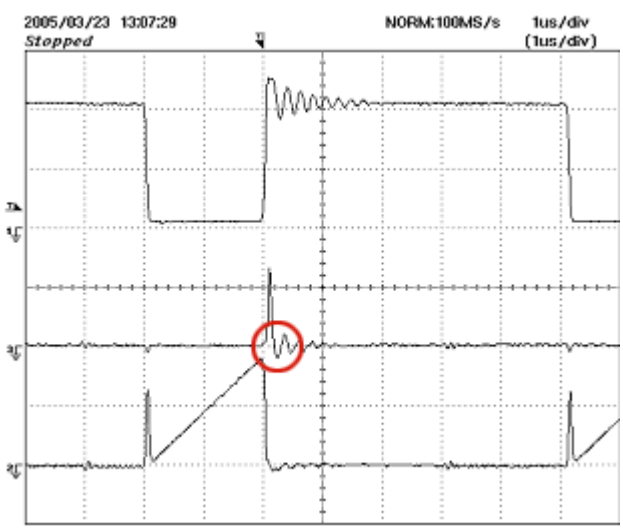
Diode reverse currents effectively recover some of the leakage inductance energy stored in the capacitance of the clamp. The longer the recovery time, the more energy is recovered.

Why?:

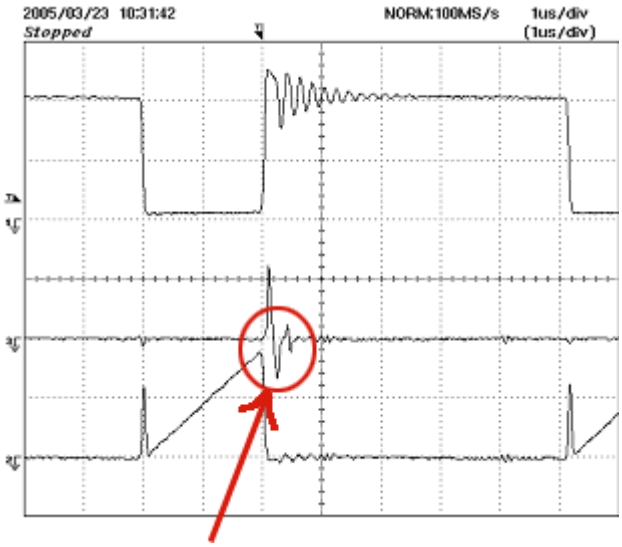
The two oscillograms below show the drain voltage (upper, 200 V/div), drain current (lower, 0.4 A/div) and the current through the clamp diode, D1, for both a UF4005 and 1N4007GP (middle, 0.4 A/div).

The slower recovery time of the 1N4007GP causes a reverse current to flow back through the primary winding at the end of the clamping period. This partially discharges the leakage energy stored in clamp capacitor, C2, and transfers some of the energy stored to the secondary, thus improving efficiency.

It might appear that the ideal diode would be very slow to maximize this effect. However, to prevent excess diode dissipation, to limit drain ringing for EMI reasons, and to prevent the drain ringing below the source at low line, the diode must have a specified recovery time. A small value series resistor is also required to limit ringing. In this case R3 acts as the damping resistor. This resistor can also be placed directly in series with D1. The 1N4007GP is a glass passivated version of the 1N4007, with a reverse recovery time specified at 2 us. The 1N4007 does not have a specified recovery time and must not be used.



UF4005



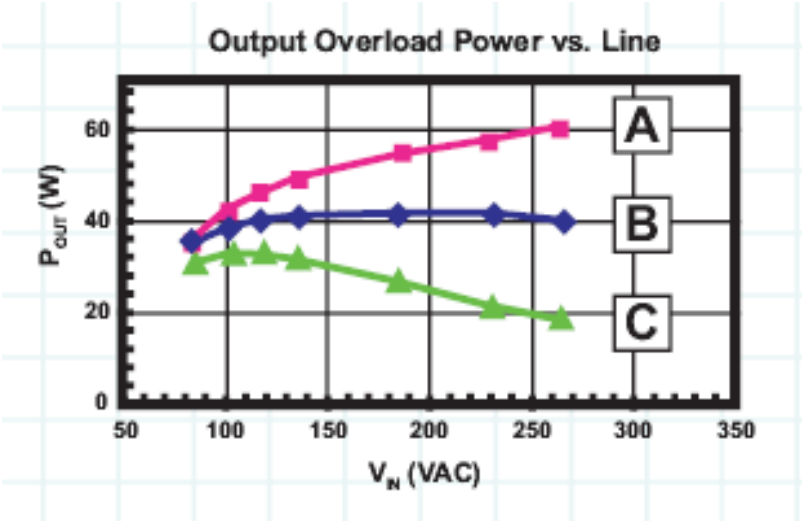
1N4007GP

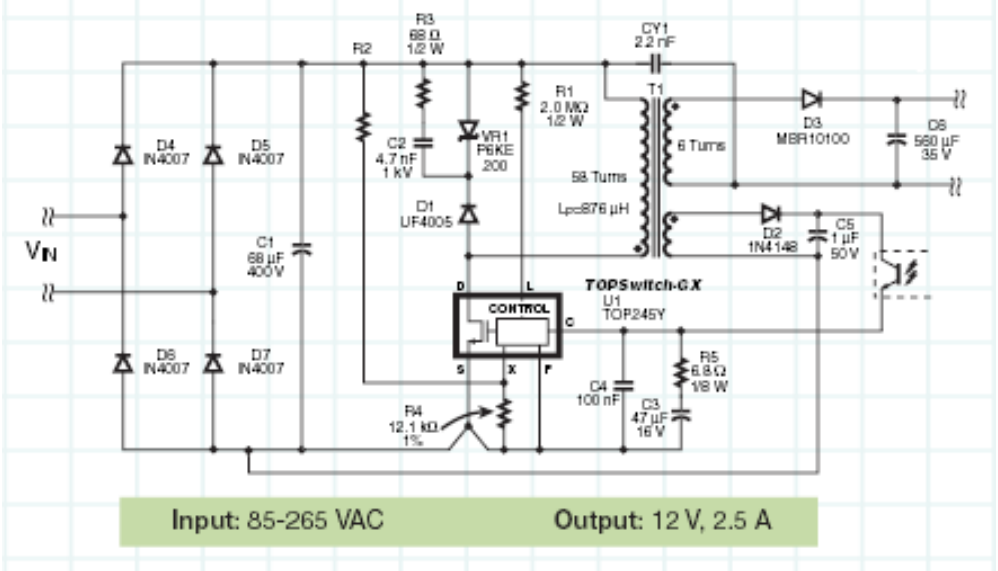
Reverse recovery current at the end of the clamp period recycles stored clamp energy to the secondary

Puzzler 2

The schematic to the right shows a flyback power supply built with a *TOPSwitch®-GX* power conversion IC. The following questions concern the output overload characteristics of the power supply.

Question 1





Which of the curves in the graph to the left (A, B or C), represent the overload characteristic of output power versus input voltage for a typical flyback power supply that is not compensated for line voltage?

Show the Answer

Answer 1

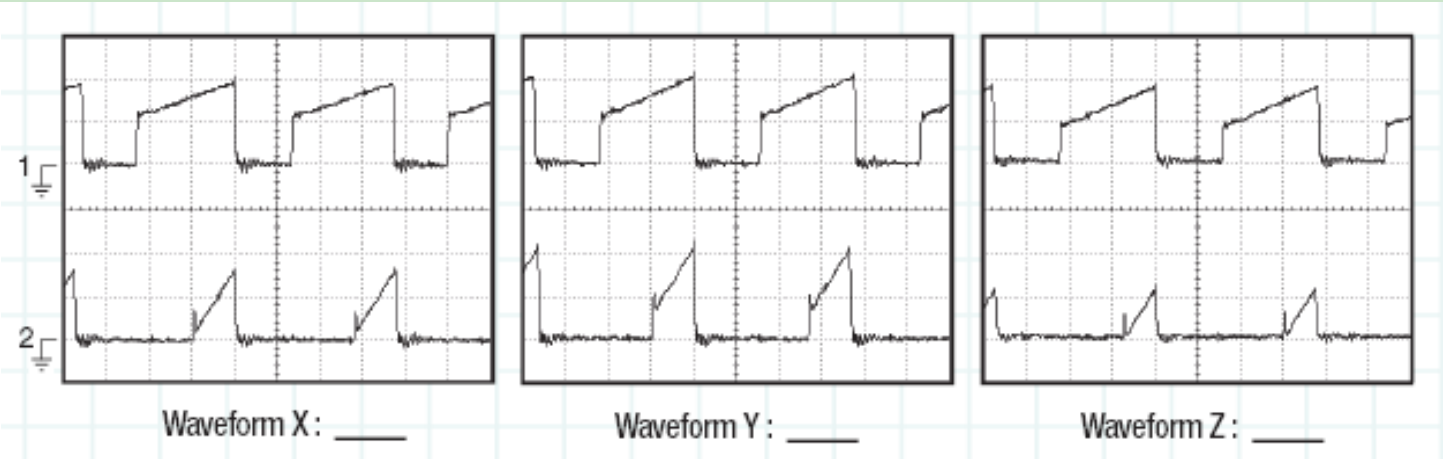
Answer is Graph A.

Why?:

The power supply used in this example is designed to deliver 12 V at 2.5 A, which equates to a nominal maximum power of 30 W. Graph A was measured with no overload power compensation. Graphs B and C were achieved by modifying the overload compensation of the power supply.

- Graph A has the typical output overload characteristic for a continuous mode flyback power supply. The output overload capability of the power supply increases significantly as input voltage increases because although the peak Drain current is controlled (I_{LIM}), the shorter duty cycle at high line allows a longer period for energy transfer. Therefore, as more energy can be transferred at high line, higher overload power results. The graph shows that the power supply is capable of delivering approximately 200 % of rated maximum output power at high input voltage (approximately 60 W) versus approximately 130% of rated maximum output power at low input voltage (approximately 40 W).
- Graph B shows a relatively flat output overload characteristic versus input line
- Graph C shows a decreased output overload characteristic versus input line

Question 2



***Test Conditions:** Upper Trace (1) V_{IN}= 85 VAC, Lower Trace (2) V_{IN}= 265 VAC, both traces 0.5 A/div, 2 µs/div Flyback drain current waveforms* X, Y and Z were taken at 85 VAC and 265 VAC. Match the waveform pairs to curves A, B and C above.

Show the Answer

Answer 2

Answer is Waveform X = B, Y = A and Z = C

Why?:

- Waveform X corresponds to a case where the output power is similar at both 85 VAC and 265 VAC input voltages. Note that in this case, the peak current is lower at 265 VAC than at 85 VAC.
- Waveform Y corresponds to a case where the output power at 265 VAC is significantly higher than that at 85 VAC. This would be the expected characteristic for a typical Flyback power supply, where the peak Drain current is set at a constant limit.
- Waveform Z corresponds to a case where the output power at 265 VAC is significantly lower than that at 85 VAC.

All the waveforms were measured on the same power supply. Upon examination of the high line (265 VAC) waveforms, it can be seen that the slopes of the current waveforms are all the same. The difference between the

waveforms is the initial and final Drain current.

The output power, (P_O), delivered to the secondary in a continuous mode flyback power supply is proportional to the difference in energy stored at the beginning and the end of the cycle. This stored energy is transferred to the secondary at the switching frequency, and thus P_O is given by the equation:

$$P_o = \frac{L_p}{2}(I_2^2 - I_1^2) f_s \eta$$

where:

- LP is the primary inductance
- I1 is the initial current
- I2 is the final peak current
- fS is the switching frequency
- ? is the power supply efficiency

This formula can be rearranged to give a value of (P_O /L_P.f_S.?) or power ratio (a_P),which is independent of primary inductance and switching frequency. For the same power supply, this power ratio (aP) can be used to calculate the relative output power of the supply.

$$a_p = \frac{P_o}{L_p \cdot f_s \cdot \eta} = \frac{(I_2^2 - I_1^2)}{2}$$

By looking at the printed waveforms we can approximate values of both the initial current (I_1) and the final peak current (I_2). From this we can calculate the value of (a_P) which gives a relative indication of output power delivered by the power supply under these conditions. We can see that the power ratio (aP) for waveform X is almost constant between low and high line. However, the power ratio for waveform Y increases dramatically at high line vs. low line. Conversely, the power ratio for waveform Z decreases significantly at high line vs. low line.

Waveform	Low Line (85 VAC)			High Line (265 VAC)		
	I_2	I_1	a_P	I_2	I_1	a_P
X	**0.90**	**0.50**	**0.28**	**0.80**	**0.20**	**0.30**
Y	**1.00**	**0.50**	**0.38**	**1.10**	**0.40**	**0.53**
Z	**0.90**	**0.45**	**0.30**	**0.65**	**0.00**	**0.21**

Question 3

It’s possible to compensate the output overload characteristic of a typical flyback power supply by controlling the peak drain current limit of the converter. When using *TOPSwitch-GX*, compensation is achieved by correctly choosing the value of just one passive component, R2 in the schematic above. What are the advantages of achieving a flat output overload characteristic?

Show the Answer

Answer 3

It is possible to control the output overload capability of a power supply by adjusting the primary peak current limit as a function of input voltage, to maintain constant output power (P_O).

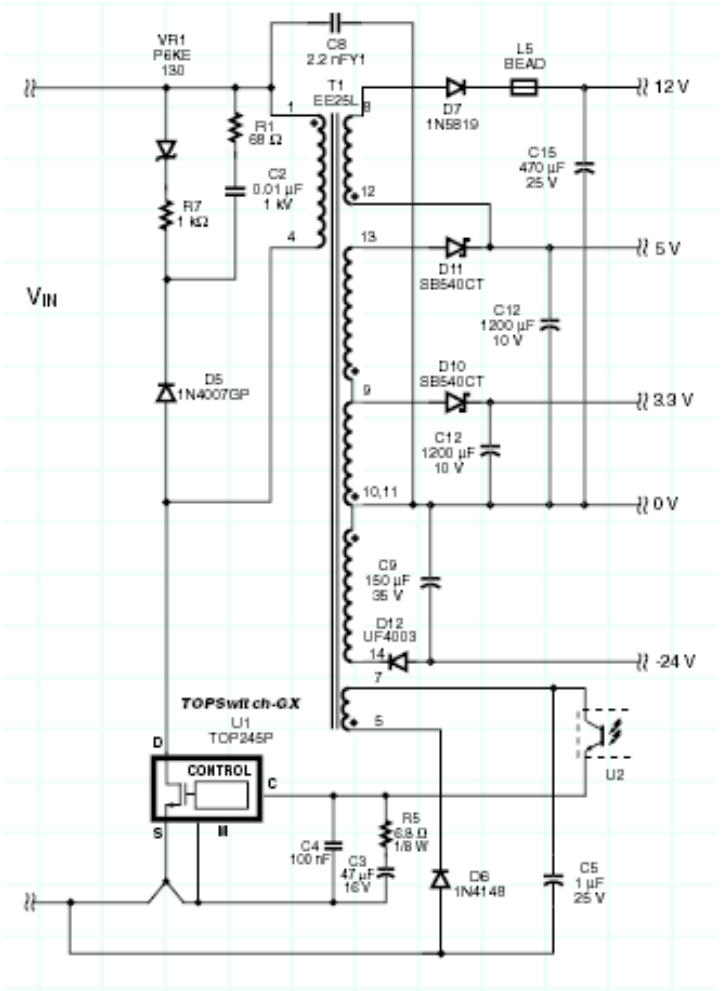
When using *TOPSwitch-GX* its possible to adjust the maximum primary peak current (I2) as a function of input voltage by controlling the input to the X-pin of the device. The resistor R2 provides this current limit adjustment as a function of input voltage. The ideal peak current control would be a non-linear adjustment. Resistor R2 provides a linear adjustment as a function of input voltage and while this is not perfect, it certainly provides an order of magnitude improvement over no compensation.

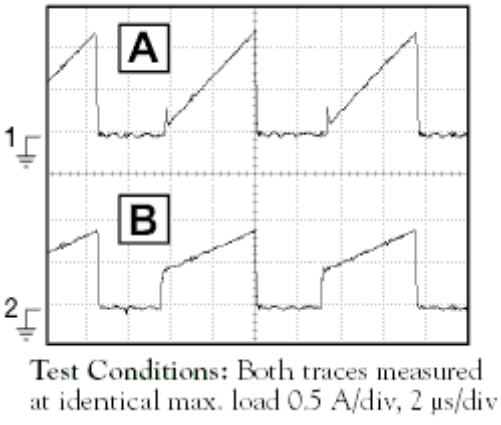
A design where the output overload characteristic is virtually flat gives the following advantages:

- When an RCD (Resistor-Capacitor-Diode) clamp is used to limit the leakage inductance spike at primary turn-off, the peak clamp voltage is a function of the peak current at the time of turn-off and the primary bus voltage. Reducing the peak Drain current at high line reduces the energy stored in the leakage inductance and reduces the clamp voltage with respect to the bus voltage, helping to preserve the margin between Drain voltage and the MOSFET breakdown voltage (BV_{DSS}) rating.
- The stress on the output diode is minimized. Without overload protection, the output diode would have to be oversized to accommodate higher peak currents and voltages during high line overloads.
- The transformer will have lower worst-case thermal stresses.
- The worst-case maximum internal dissipation of the power supply during overload is reduced. This can be an important consideration for power supplies in small enclosures where self-heating of the power supply can be a problem (such as laptop or other adapters).

Puzzler 3

Take a break from your daily routine and test your power supply design knowledge by answering the three questions below regarding continuous conduction mode operation in multiple output supplies.
The schematic shows a typical multi-output flyback power supply built with a *TOPSwitch®-GX* power conversion IC. The following questions concern deeply continuous mode of operation.





Test Conditions: Both traces measured at identical max. load 0.5 A/div, 2 µs/div

Question 1

The Drain current waveforms A and B were measured in an identical power supply except for a different transformer primary inductance. Table 1 contains both the rms and peak current values.

1. Identify the peak current for waveforms A and B from the values (W, X, Y and Z)
2. Identify the rms current for waveforms A and B from the values (W, X, Y and Z)
3. Which is more important for efficiency - peak current or rms current?

W	X	Y	Z
0.568 A	0.88 A	1.2 A	0.538 A

Table 1 - Different (rms) and (peak) currents

Show the Answer

Answer 1

The Correct Answer:

a. Waveform A Ipk = Y (1.2 A). Waveform B Ipk=X (0.88 A).

This can be directly measured from the printed waveform.

b. Waveform A Irms = W (0.568 A). Waveform B Irms = Z (0.538 A).

The rms current can be calculated as follows:

RMS and Peak Current Calculation

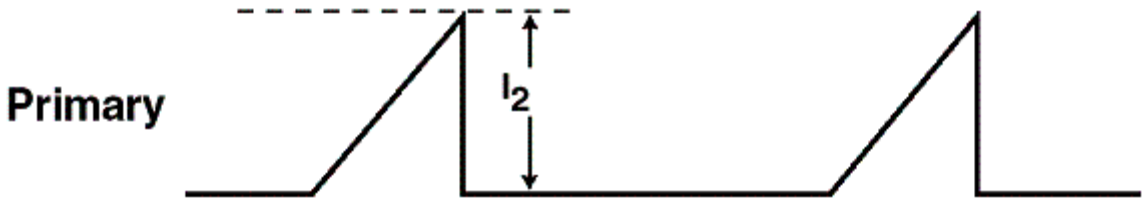


Figure 2 - Primary Current - Borderline Continuous/Discontinuous, Kp ³ 1

The formula below gives the value of RMS current when operating in discontinuous or borderline continuous/discontinuous modes:

$$I_{RMS} = I_2 \cdot \sqrt{\frac{D_{ON}}{3}}$$

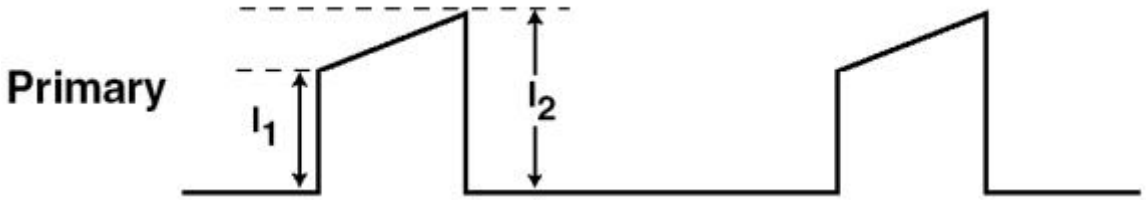


Figure 3 - Primary Current - Continuous, Kp < 1

The formula below gives the value of RMS current when operating in continuous mode:

$$I_{RMS} = \sqrt{\frac{1}{T} \cdot \int_0^{Ton} I^2(t) \cdot dt}$$

$$I(t) = I_1 + \frac{(I_2 - I_1)}{T_{ON}} \cdot t$$

$$I^2(t) = {I_1}^2 + 2 \cdot (I_2 - I_1) \cdot \frac{I_1}{T_{ON}} \cdot t + \frac{(I_2 - I_1)^2}{{T_{ON}}^2} \cdot t^2$$

$$\int_0^{T_{ON}} I^2(t) \cdot dt = \left[{I_1}^2 \cdot t + (I_2 - I_1) \cdot \frac{I_1}{T_{ON}} \cdot t^2 + \frac{(I_2 - I_1)^2}{3 \cdot {T_{ON}}^2} \cdot t^3 \right]_0^{T_{ON}}$$

$$\int_0^{T_{ON}} I^2(t) \cdot dt = T_{ON} \cdot \left[\frac{{I_1}^2}{3} + \frac{I_1 \cdot I_2}{3} + \frac{{I_2}^2}{3} \right]$$

$$I_{RMS} = \sqrt{\frac{D_{ON}}{3} \cdot \left[{I_1}^2 + I_1 \cdot I_2 + {I_2}^2 \right]} \qquad \text{Where } D_{ON} = \frac{T_{ON}}{T}$$

Using this formula along with the measurement data from the primary current waveforms, we are able to calculate the RMS currents for both waveforms. Please note that Waveform A is very slightly continuous - this can be seen from the non-zero initial current in this waveform. Hence the continuous mode formula should be used for RMS calculations with both waveforms A and B.

Table 4 - Waveform A and B - Measurement Data				
	T_{ON}	T	I_1	I_2
Wvfm A - read from waveform	4.35E-06	7.50E-06	0.099	1.239
Wvfm B - read from waveform	4.45E-06	7.52E-06	0.497	0.882

c. Both RMS and peak currents affect the efficiency. The peak current determines the parasitic losses in the leakage inductance (1/2.L.Ipk²). The RMS current determines the loss in resistive elements such as the primary MOSFET ($I_{RMS^2.\ rds(ON)}$), along with resistive elements in the power supply. It can be seen that by running in continuous conduction mode the RMS currents are significantly reduced (bear in mind that the resistive losses are proportional to the square of the RMS current - hence even a small increase can be significant when calculated out).
For instance in the power supply in question, the efficiencies with waveforms A and B were as follows:

Table 6 - Waveform A and B - Power Supply Efficiency		
Waveform	**A**	**B**
Efficiency	69.1%	73.7%

This example shows that it only takes a small reduction in RMS switching currents to give a large improvement in power supply efficiency.

Question 2

Table 2 - Percentage regulation (±) on the different outputs from min. to max. load				
Output	**3.3 V**	**5 V**	**12 V**	**-24 V**
P	2.90%	5.80%	5.10%	6.05%
Q	4.55%	9.50%	7.90%	7.80%

Match the waveforms A and B with the cross-regulation performance data (P and Q)
Why does a change in primary inductance cause cross-regulation performance to change?

Show the Answer

Answer 2

Output	3.3 V	5 V	12 V	24 V	Mode	Waveform
P	2.90%	5.80%	5.10%	6.05%	Deeply Continuous	B
Q	4.55%	9.50%	7.90%	7.80%	Mostly Discontinuous	A

Table 7 – Waveform A and B – Percentage Regulation (±) from Min. to Max. Loads

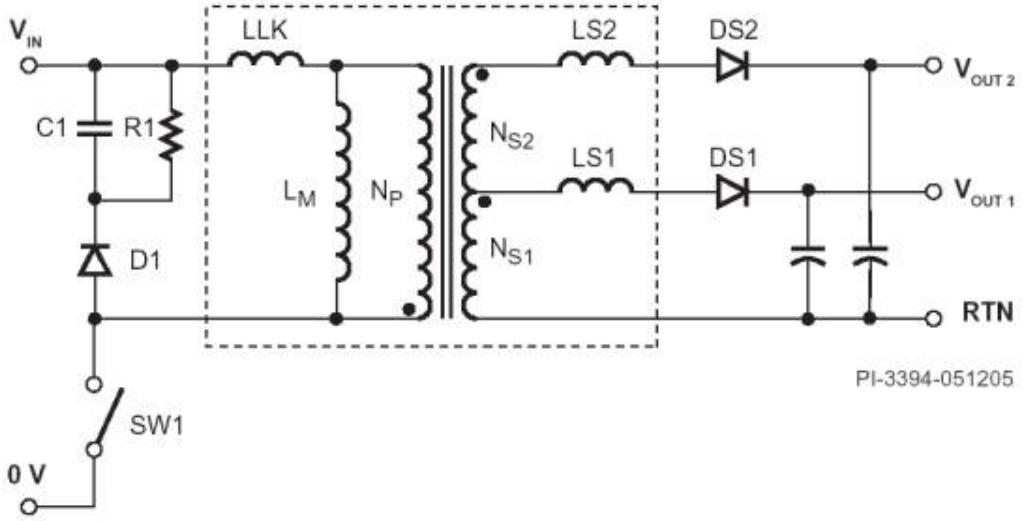


Figure 8 – Schematic of Transformer Model for a Multi-Output Power Supply

Continuous, K P < 1 Discontinuous, K P ≥ 1

Figure 8b Example of secondary current waveform

The above is a model of the inductances in a multiple output flyback transformer, showing the following transformer parameters:

LM – magnetizing (main) inductance

LLK – primary leakage inductance – the voltage spike caused by this leakage inductance is limited by the clamp network (D1, C1 and R1)

LS1 – secondary output 1 leakage inductance

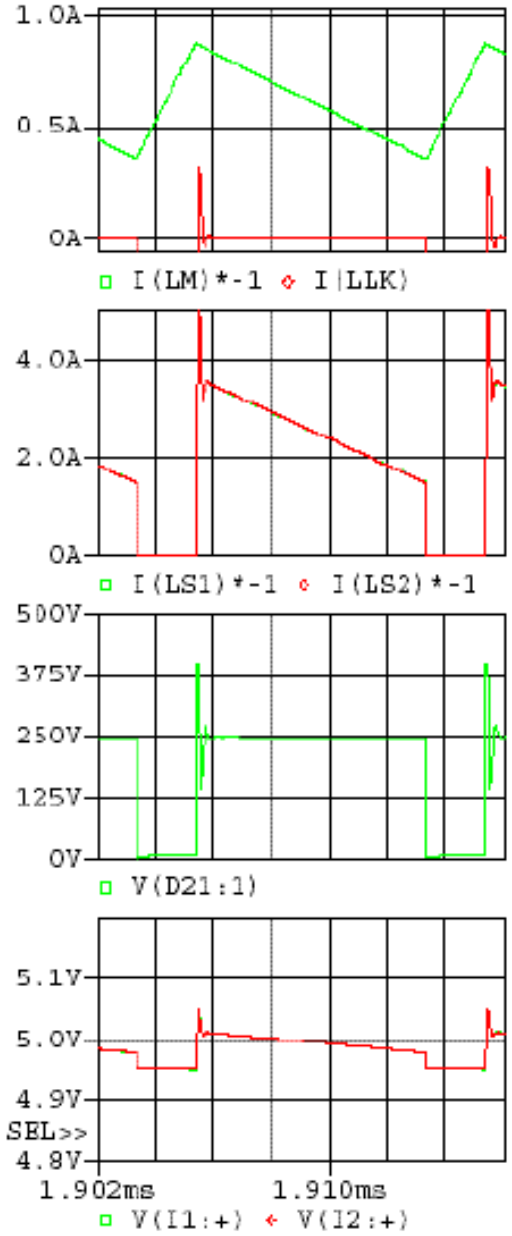
LS2 – secondary output 2 leakage inductance

During primary switch (SW1) conduction, equal current will ramp up both in LM and LLK. When the primary switch turns off, the voltage across LM is limited while LLK resets and current discharges into the primary clamp network (R1, C1 and D1). Once LLK is reset , the remaining energy from LM is delivered to the secondary. As this is a Flyback topology , the secondary winding current starts from zero at the point SW1 turns-off (figure 8b) and a voltage is developed across LS1 and LS2 caused by the high ΔI. This voltage causes an error between the outputs dependant on the peak secondary current which is in turn dependant on the output load and operating mode. As continuous conduction mode designs have lower peak secondary currents this error is minimized giving better cross regulation.

The waveforms shown below are from a simulation of a power supply with two identical 5 V outputs. Results are shown for two transformers, one with higher inductance (operating in deeply continuous conduction mode) and the second with lower inductance (operating in discontinuous conduction mode).

It can be clearly seen from the bottom waveform in each set of plots, that the two output voltages V_{OUT1} and V_{OUT2} diverge when the outputs are loaded differently (one at min. load the other at max. load as shown in figures 11 to 14). This is due to the different in voltage drop on the respective secondary leakage inductances. It can also be seen that the **regulation difference significantly better with the deeply continuous mode supply (due to lower di/dt and peak currents)**.

Note: when both outputs are loaded at the same current (figures 9,10, 15 and 16), there will be no difference in regulation, since both secondary leakage inductances will have the same voltage drop.



I_{LM}, I_{LLK}

I_{LS1}, I_{LS2}

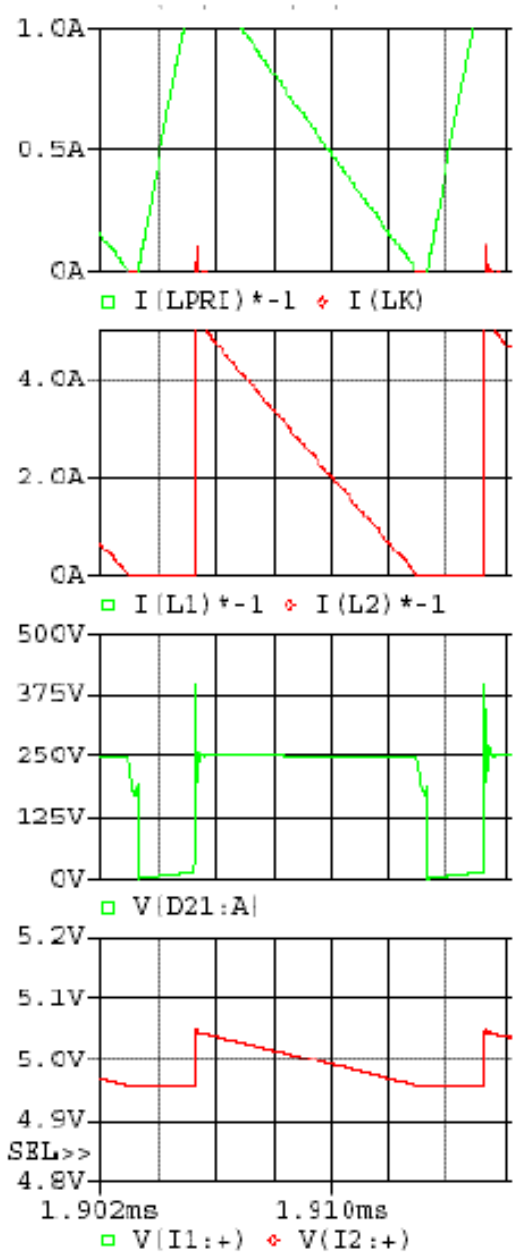
Note: Lower ΔI for continuous mode

V_{DRAIN}

V_{OUT1}, V_{OUT2}

Note: Identical regulation when both loads the same (full-load)

Figure 9 – Deeply Continuous Mode
I_{OUT1} and I_{OUT2} = 2 Amps
Upper: I_M, I_{LK}, 0.5 A/ div,
Mid-Upper: I_{LS1}, I_{LS2}, 2 A/ div,
Mid-Lower: V_{DRAIN}, 125 V/ div,
Lower: V_{OUT1}, V_{OUT2} 0.1 V, 2 µs / div



Note: High ΔI for discontinuous mode

Note: Identical regulation even for discontinuous when both loads the same (full-load)

Figure 10 – Discontinuous Mode
I_{OUT1} and I_{OUT2} = 2 Amps
Upper: I_M, I_{LK}, 0.5 A/ div,
Mid-Upper: I_{LS1}, I_{LS2}, 2 A/ div,
Mid-Lower: V_{DRAIN}, 125 V/ div,
Lower: V_{OUT1}, V_{OUT2} 0.1 V, 2 µs / div

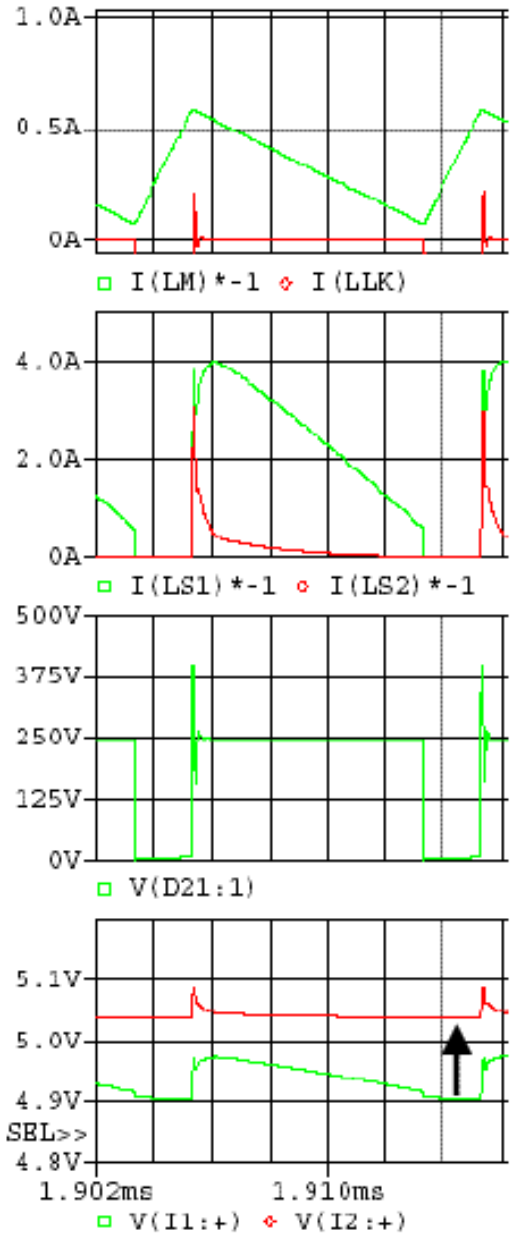


Figure 11 - Deeply Continuous Mode
I_{OUT1} = 2 Amps and I_{OUT2} = 0.1 Amps
Upper: I_M,I_{LK}, 0.5 A/ div,
Mid-Upper: I_{LS1},I_{LS2}, 2 A/ div,
Mid-Lower: V_{DRAIN}, 125 V/ div,
Lower: V_{OUT1}, V_{OUT2} 0.1 V, 2 µs / div

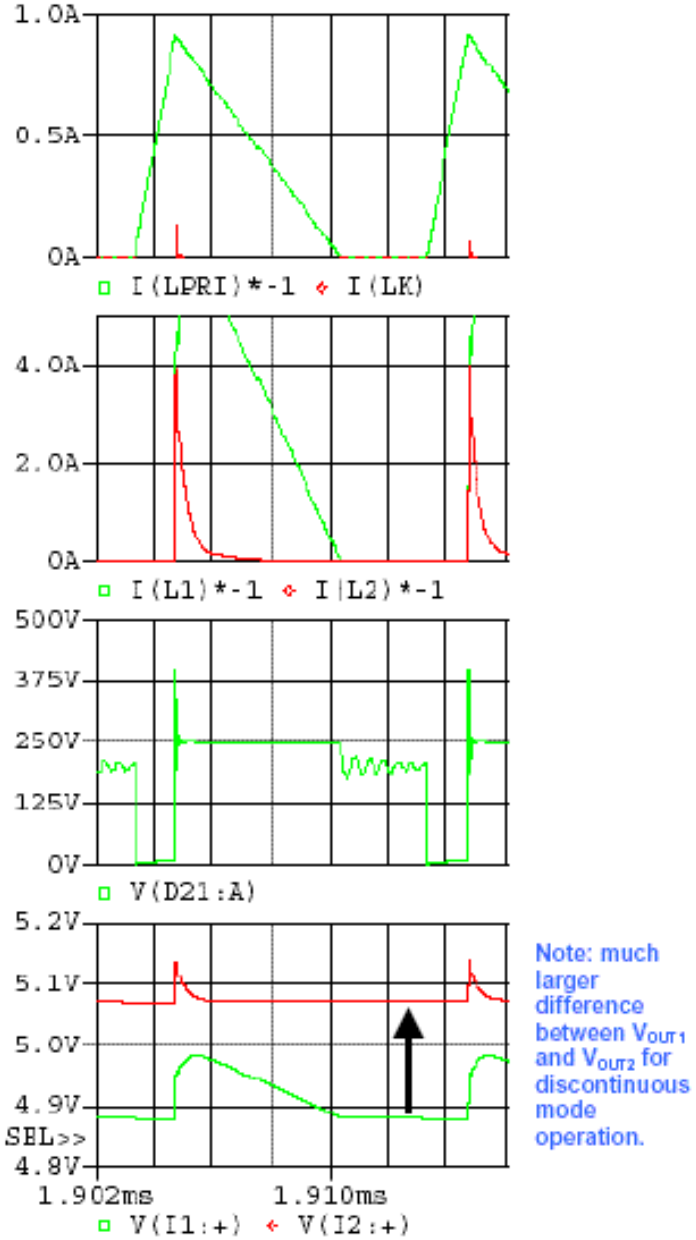


Figure 12 - Discontinuous Mode
I_{OUT1} = 2 Amps and I_{OUT2} = 0.1 Amps
Upper: I_M,I_{LK}, 0.5 A/ div,
Mid-Upper: I_{LS1},I_{LS2}, 2 A/ div,
Mid-Lower: V_{DRAIN}, 125 V/ div,
Lower: V_{OUT1}, V_{OUT2} 0.1 V, 2 µs / div

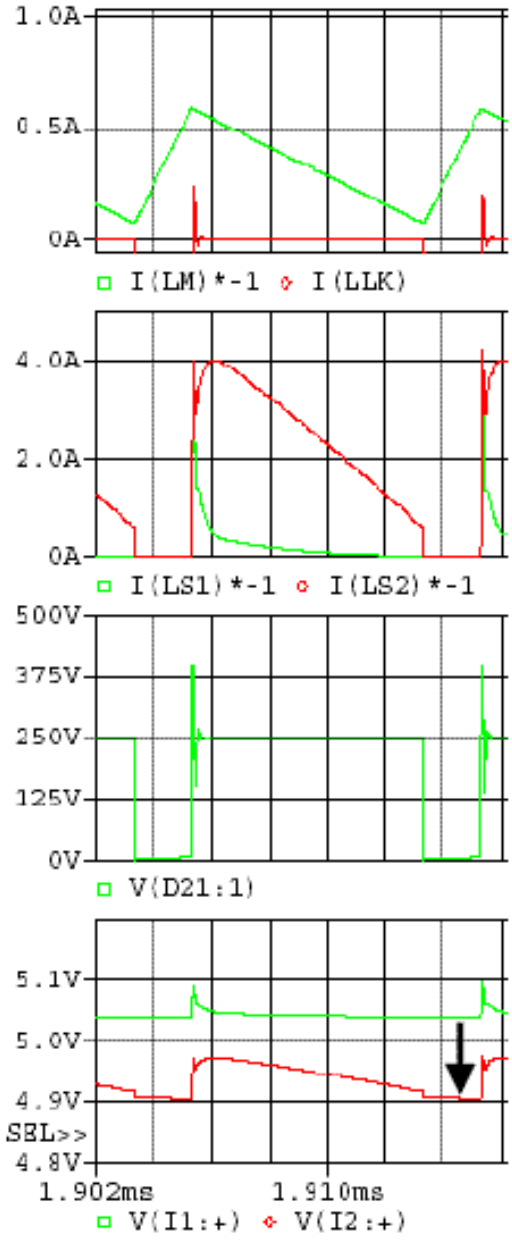


Figure 13 - Deeply Continuous Mode
I_{OUT1} = 0.1 Amps and I_{OUT2} = 2 Amps
Upper: I_M,I_{LK}, 0.5 A/ div,
Mid-Upper: I_{LS1},I_{LS2}, 2 A/ div,
Mid-Lower: V_{DRAIN}, 125 V/ div,
Lower: V_{OUT1}, V_{OUT2} 0.1 V, 2 µs / div

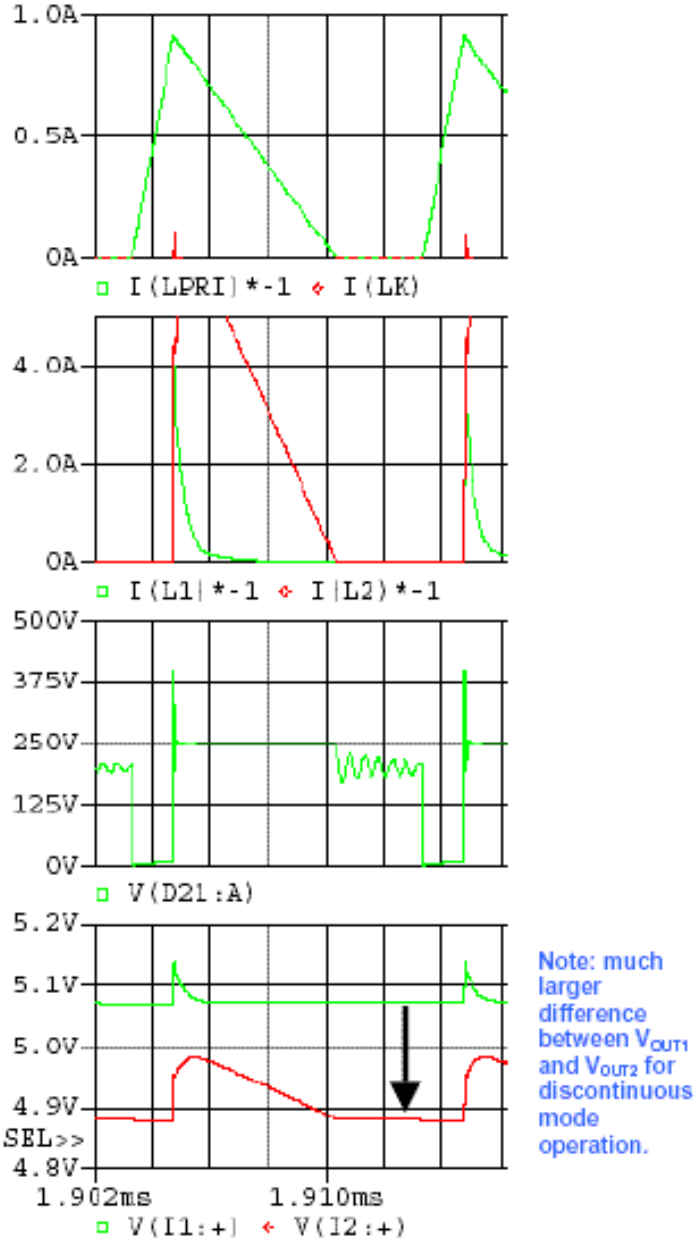


Figure 14 - Discontinuous Mode
I_{OUT1} = 0.1 Amps and I_{OUT2} = 2 Amps
Upper: I_M,I_{LK}, 0.5 A/ div,
Mid-Upper: I_{LS1},I_{LS2}, 2 A/ div,
Mid-Lower: V_{DRAIN}, 125 V/ div,
Lower: V_{OUT1}, V_{OUT2} 0.1 V, 2 µs / div

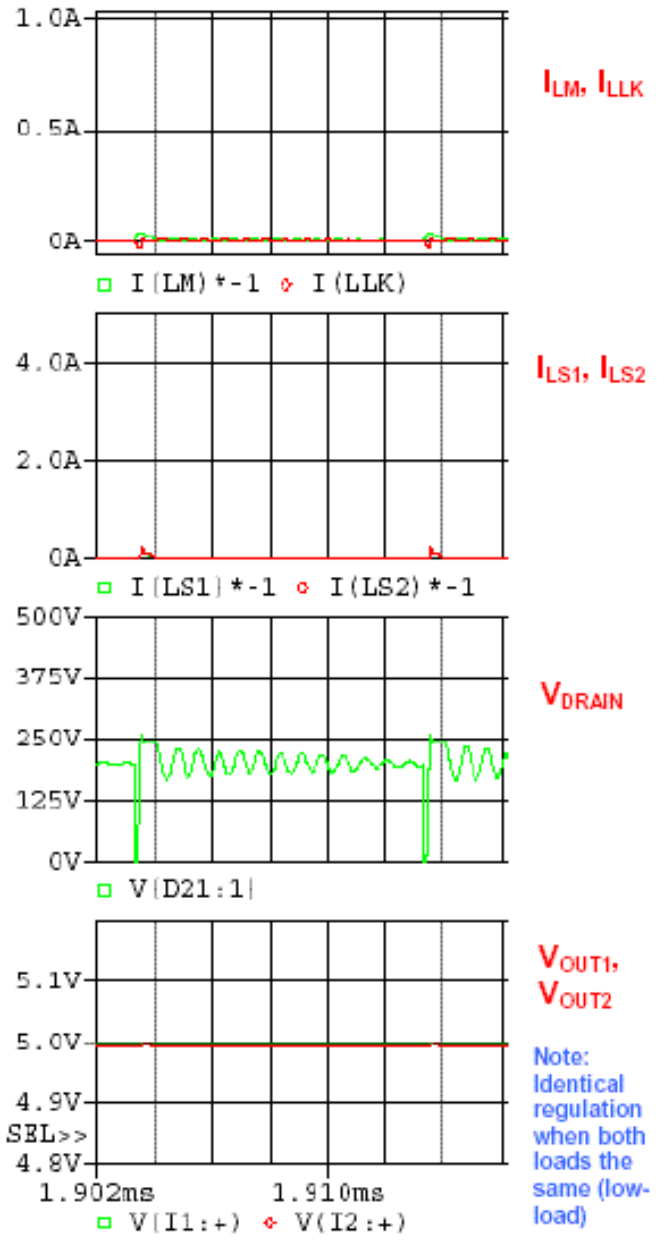


Figure 15 - Deeply Continuous Mode
I_{OUT1} = 0.1 Amps and I_{OUT2} = 0.1 Amps
Upper: I_M, I_{LK}, 0.5 A/ div,
Mid-Upper: I_{LS1}, I_{LS2}, 2 A/ div,
Mid-Lower: V_{DRAIN}, 125 V/ div,
Lower: V_{OUT1}, V_{OUT2} 0.1 V, 2 µs / div

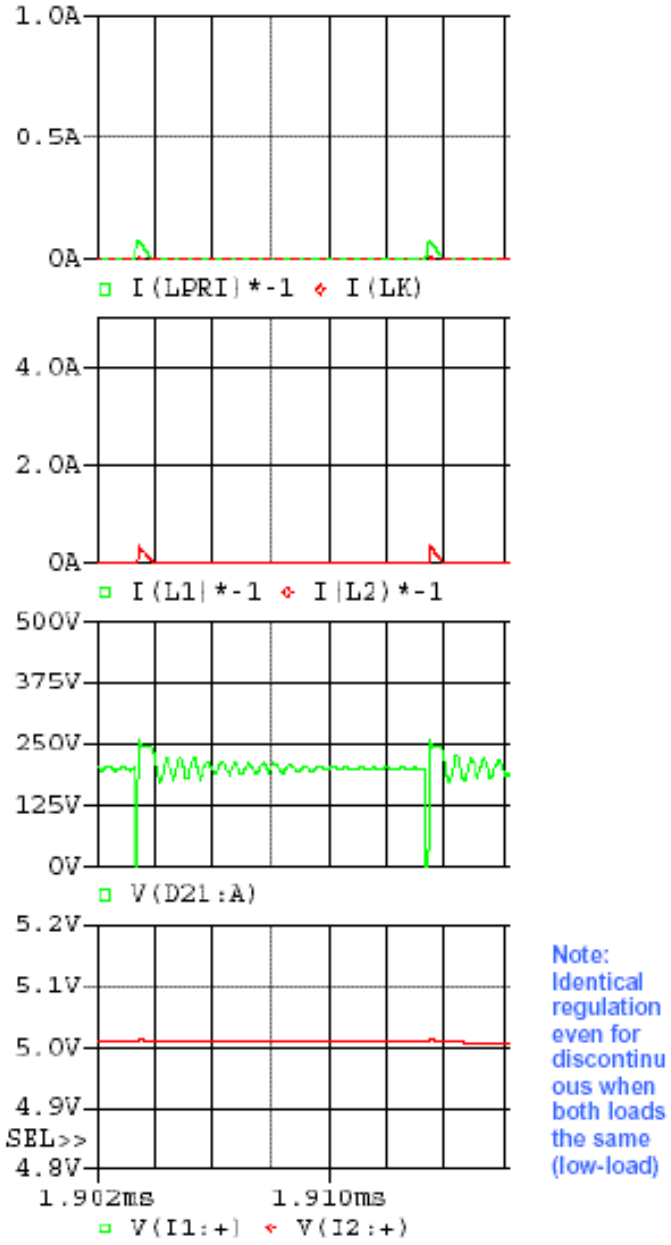


Figure 16 - Discontinuous Mode
I_{OUT1} = 0.1 Amps and I_{OUT2} = 0.1 Amps
Upper: I_M, I_{LK}, 0.5 A/ div,
Mid-Upper: I_{LS1}, I_{LS2}, 2 A/ div,
Mid-Lower: V_{DRAIN}, 125 V/ div,
Lower: V_{OUT1}, V_{OUT2} 0.1 V, 2 µs / div

Question 3

What are the major advantages of continuous conversion mode operation for multiple output power supplies? How is voltage-mode control different from current-mode control in its ability to run in deeply continuous conduction mode?

Show the Answer

Answer 3

Continuous conduction mode has the following major advantages:

- Lower RMS currents yield higher efficiency
- Lower peak currents lead to better cross regulation in multiple output designs
- Lower peak currents also lead to better differential mode conducted (and radiated) EMI performance (or smaller input capacitors).
- Lower peak and RMS currents contribute to better output ripple (or smaller output capacitors)

- Continuous mode operation gives higher loop gain and therefore has faster transient response than discontinuous mode

In it's basic form current mode cannot go beyond 50% duty cycle without risk of instability. A maximum duty cycle limit of 50 % causes peak currents to be higher for a given power level than if the duty cycle were allowed to increase. It is possible to overcome the 50% duty cycle limit by using slope compensation but this requires careful choice of components.

Conversely Voltage mode in its basic form, does not have a limitation on maximum duty cycle. This allows deeply continuous voltage mode designs providing their inherent advantages.

Puzzler 4

Take a break from your daily routine and test your power supply design knowledge by answering the three questions below regarding new mandatory energy efficiency requirements.

Question 1

Recent energy efficiency regulations set minimum standards for the efficiency and no-load power consumption of certain AC-DC and AC-AC power supplies. In China and Europe, minimum energy efficiency targets are already in place and in several U.S. states, regulations are becoming mandatory. The California Energy Commission (CEC) has set mandatory requirements for external power supplies (EPS) sold in California from July 2006. Which of the following is true? CEC requires that:

1. EPS rated at under 10 W should consume less than 0.5 W under no-load conditions
2. EPS rated at 10 W to 250 W should consume less than 0.75 W under no-load conditions
3. An Active Mode minimum efficiency must be met, based upon the average of the efficiencies at 25%, 50%, 75% and 100% load
4. All of the above

(Hint: Visit the Green Room)

Show the Answer

Answer 1

The answer is (d) – All of the above.

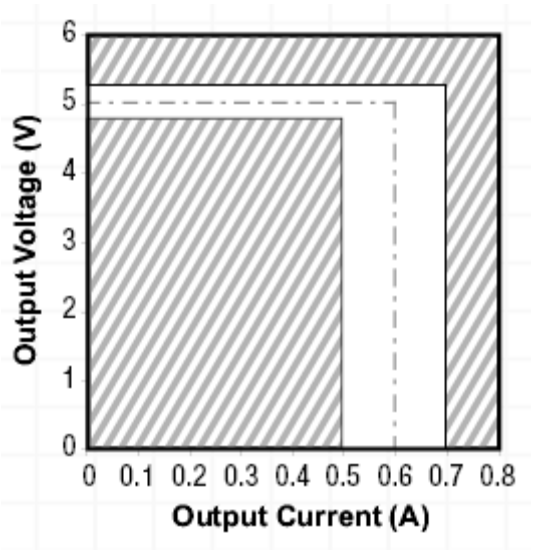
Many countries and individual states within the USA are in the process of adopting, or have already adopted new energy efficiency regulations, covering wide ranges of electrical equipment. To find the latest regulations, including the recent mandatory California Energy Commission regulations, visit the Regulations by Location page for hyperlinks to all the major agency energy standards worldwide.

Want to check if your EPS design meets the CEC requirements? Try using the CEC calculator.

Simply enter the rated output power (per the product label), the measured no-load power consumption and the measured efficiency at the 25%, 50%, 75% and 100% of the rated output power at 115 VAC, and, if applicable, 230 VAC. The calculator will tell you the CEC requirements, compute the average efficiency of your EPS, and indicate whether your design will pass.

For a wide range of examples of power supply designs that meet the CEC requirements, visit the Design Examples page.

Question 2



A 3 W, 5 V CV/CC charger requires the characteristics as shown:

Which is the best choice of power supply to meet CEC no-load requirements and why?

1. A linear transformer with an IC linear post regulator
2. A Switched Mode Power Supply (SMPS) designed using discrete components, with a characteristic of increasing frequency at light loads
3. An SMPS designed using an IC that operates at a fixed frequency
4. An SMPS designed using an IC with a characteristic of decreasing frequency at light loads

Show the Answer

Answer 2

The answer is (d) - an SMPS designed using an IC with a characteristic of decreasing frequency at light load. Maintaining high switching frequency operation at light loads results in high switching losses, thereby increasing no-load consumption and decreasing light load efficiency. PI devices utilize *EcoSmart*® technology, reducing the operating frequency as load decreases. This maintains an optimum balance of switching losses to conduction losses, so that the best overall efficiency is obtained.

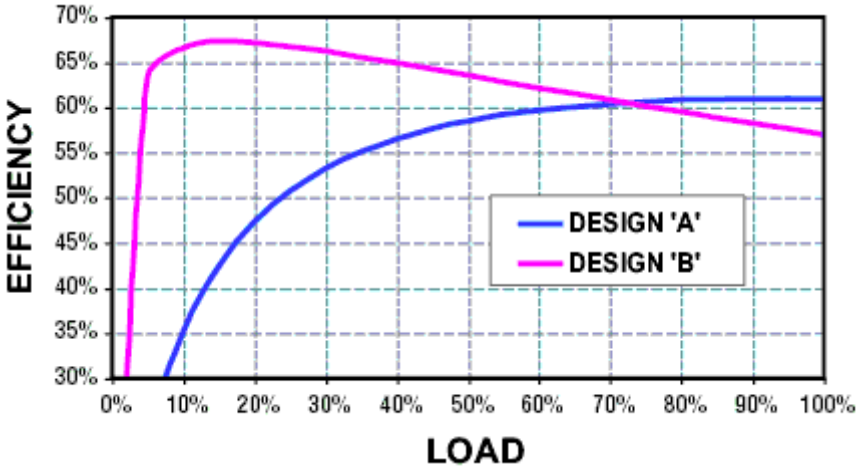
Using a linear transformer with an IC linear post regulator (a), it would be extremely difficult to meet the CEC requirements, as firstly the no-load consumption is relatively high for linear transformers due to losses in the iron core, and secondly the regulation efficiency for a linear system is very poor. Consequently, such a design is unlikely to meet either no-load or the average efficiency requirement.

Designing a Switched Mode Power Supply (SMPS) using discrete components (b), with a characteristic of increasing frequency at light loads, would also be very a challenging prospect. The typical ‘Ringing Choke Converter’ (RCC) type discrete power supply has characteristics similar to this. Such discrete supplies may appear to be low cost on paper, but the high component count and associated wide tolerances cause major difficulties in meeting and maintaining the levels of no-load and efficiency required to meet CEC. Also, the inherent effect of increasing frequency at light loads tends to increase the proportion of switching losses at low power levels. Consequently, as the load is reduced, a higher proportion of processed power is dissipated through switching losses, particularly impacting the 25% and 50% efficiency levels, making it hard to meet the overall average efficiency requirement.

An SMPS designed using an IC that operates at a fixed frequency (c) also suffers from similar problems to (b). Without frequency reduction, switching losses become dominant at light loads, impacting efficiency and subsequently the overall average efficiency performance. While integration generally brings component reduction, not all integrated devices are the same; PI devices offer the best integrated solutions to meet existing and emerging energy regulation requirements.

Question 3

The CEC Active Mode minimum efficiency requirement for a 3 W, 5 V output EPS is 58.9%. The CEC also requires less than 500 mW no-load consumption at this rated output power level.



For your 3 W, 5 V CEC-compliant charger, two designs points, ‘A’ and ‘B’, are being considered, with efficiency versus load characteristics as shown in the figure. Which would be a better choice to meet the CEC requirements and why?

1、 DESIGN ‘A’: an SMPS with 450 mW no-load consumption and 100% load efficiency of 61%

2、 DESIGN ‘B’: an SMPS with 30 mW no-load consumption and 100% load efficiency of 57%

Show the Answer

Answer 3

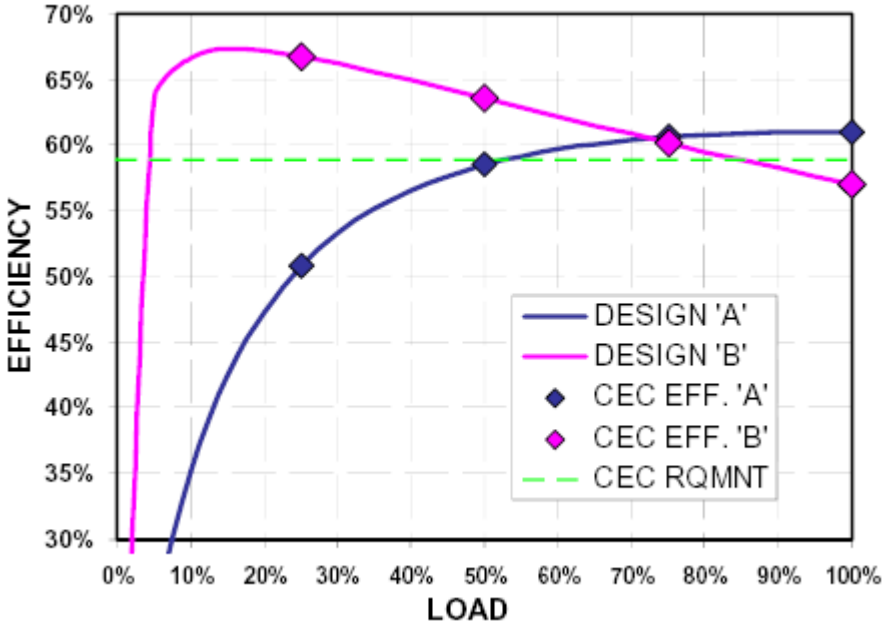
From the description, it might appear that design ‘A’ may be a better choice of charger to meet the CEC requirements, as it has 450 mW no-load consumption and 100% load efficiency of 61%, which appear to be within the CEC requirements of 58.9% average efficiency and less than 500 mW no-load consumption at this rated output power level.

However, the CEC active mode efficiency requirement *is an average of the 25%, 50%,75% and 100% efficiencies* at the rated output at 115 VAC or 230 VAC, whichever is worse (or applicable). In fact, taking measurements from the graph, as per Table 1 below, shows that Design ‘A’ only achieves an average of 57.7%, failing to meet the CEC requirement of 58.9% by more than 1%.

	25%	50%	75%	100%	CEC AVE
DESIGN 'A'	50.8%	58.5%	60.6%	61.0%	**57.7%**
DESIGN 'B'	66.5%	62.6%	60.1%	56.9%	**61.5%**

Table 1. CEC EFFICIENCIES OF DESIGN ‘A’ AND DESIGN ‘B’

Design ‘B’, on the other hand, is based on a *TinySwitch®-II* TNY264 design, optimized for ultra low 30 mW no-load consumption. Full details of this actual design, including bench measurements and construction information can be found in PI Design Idea DI-84 and Engineering Prototype Report EPR-84. While the 100% load efficiency measurement is slightly below the CEC average active mode requirement, it can be seen from Table 1 that the overall average of 61.5% has a 2.6% margin to the CEC specification. In addition, it has world-class no-load efficiency of less than 30 mW, yet component count and cost are very similar to any typical low cost *TinySwitch* charger circuit.



TinySwitch-II circuits can achieve such high light load efficiency because *EcoSmart*® technology automatically reduces the frequency of operation at light loads as a result of the On/Off regulation system, only switching to provide a power pulse when required. Consequently, switching losses are reduced to a minimum.
In addition, *TinySwitch-II* devices can be powered by either an internal current source or an external bias supply. No-load consumption of less than 300 mW can easily be achieved using the internal current source (without the use of an external bias winding), but for ultra low consumption circuits, such as DI-84, an external bias winding is used to provide the very small supply current required for normal operation.

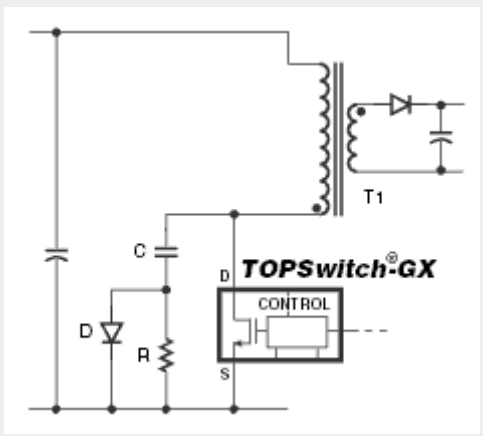
Puzzler 5

Limiting the maximum drain voltage that your power switch sees is essential to ensure its reliable operation. Take a break from your daily routine and test your power supply design knowledge by trying your hand at answering the three questions below regarding circuits designed to control the drain voltage of switched mode power supplies.

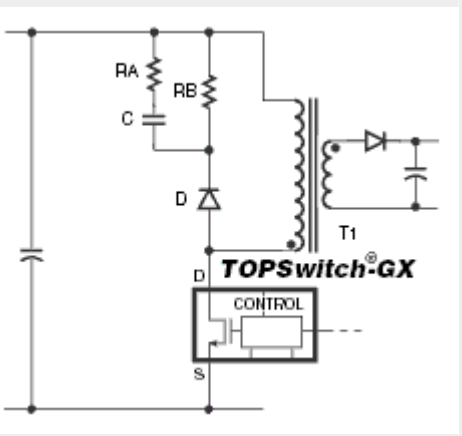
Question 1

In the figure below, choose which circuit best matches the stated requirement:

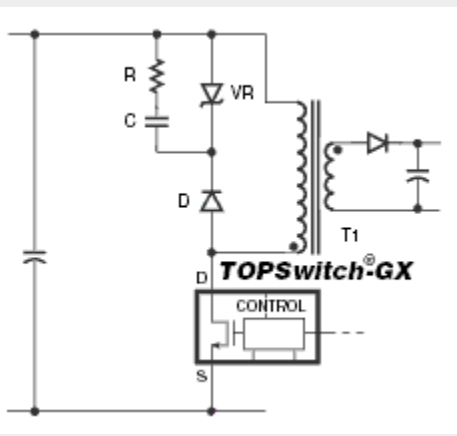
1. A low-cost clamp circuit to efficiently limit the maximum drain voltage
2. A well controlled clamp circuit to limit the maximum drain voltage while also giving the lowest no-load consumption and best efficiency
3. A circuit that can be used either to clamp the drain voltage or to limit the rate of rise of the drain voltage at turn off



(A)



(B)

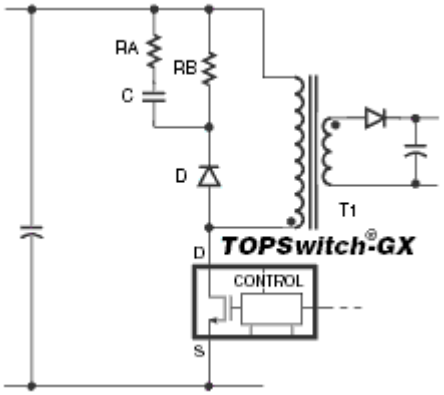


(C)

Show the Answer

Answer 1

a) A low-cost clamp circuit to efficiently limit the maximum drain voltage



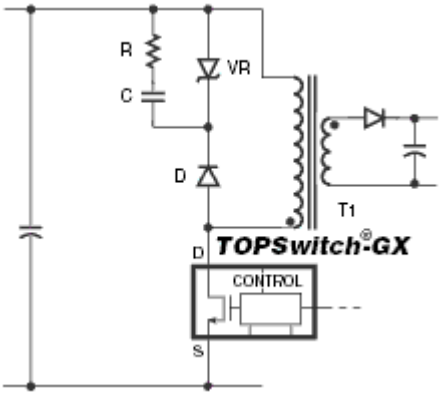
The lowest cost approach to dissipating leakage inductance energy is to provide a diode clamp to an RC network, as in circuit 'B'. Such circuits are known as 'Resistor-Capacitor-Diode' (RCD) clamps.

The energy in the leakage inductance will drive the drain voltage high until it becomes greater than the voltage stored in the clamp capacitor C, at which point the diode conducts and the drain is clamped. The resistor RB is chosen such that the energy it dissipates at the nominal clamp voltage, V_{CLO}, is equal to the energy stored in the clamp capacitor every cycle. V_{CLO} is normally set at approximately 50% higher than the reflected output voltage, V_{OR}.

The value of resistor RA is chosen to limit the reverse current in order to prevent the clamp diode 'snapping off', which in turn may cause excessive ringing and lead to EMI problems. It also slows the rise of current in clamp diode D, again limiting EMI generation, and allowing the maximum clamp voltage to be impressed across the leakage inductance for fastest and most efficient depletion of its energy.

Due to its low cost, circuit 'B' is most often used as a drain clamp. Care has to be taken in the design though, because the clamp voltage is a function of many component tolerances and operational variables (see the answer to question 3).

b) A well controlled clamp circuit to limit the maximum drain voltage while also giving the lowest no-load consumption and best efficiency



Circuit 'C' is a well controlled clamp circuit that accurately limits the maximum Drain voltage, while also giving the lowest no-load consumption and best efficiency.

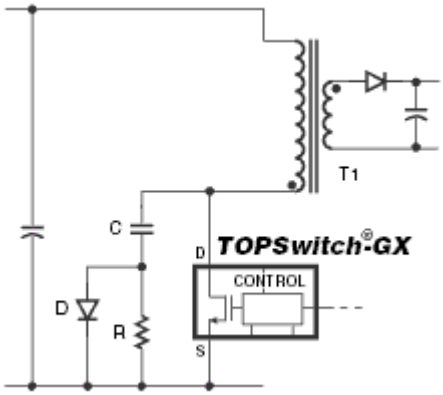
Using a zener or Transient Voltage Suppressor (TVS) device accurately sets the clamp voltage, V_{CLO}, to a specified level, making the maximum clamp voltage much less dependent upon component tolerances and operational variables.

The circuit has lower no-load consumption because when the stored capacitor voltage drops below the threshold of VR, it no longer dissipates energy. By contrast, an RCD clamp continues to discharge, dissipating energy that then has to be restored during the next cycle, robbing energy from the secondary, hence leading to higher losses than are necessary.

The capacitor and series resistor are used to lower the impedance to the pulsed clamp current, and also allow for a small reservoir for any charge extraction during the reverse current flow period when the clamp diode turns off. This helps to lower clamp losses even further, and allows very low no-load and standby power consumption. An example of a very low no-load circuit using a TVS clamp is demonstrated in the 3 W output, 30 mW no-load power charger design using the *TinySwitch-II* device TNY264 in reference design report EPR-84 (see Design Examples).

While the zener or TVS clamp is preferable from a functional perspective, the circuit is slightly more expensive than an RCD clamp.

c) A circuit that can be used either to clamp the drain voltage or to limit the rate of rise of the drain voltage at turn off



Circuit 'A' is a circuit that can be used either to clamp the drain voltage or to limit the rate of rise of the drain voltage at turn off.

While it contains basically the same components as the RCD clamp in figure 'B', there is a critical difference in that any energy stored on capacitor C must be supplied from the supply rail during turn off. In circuit 'B', current used to charge the clamp capacitor flows in a loop that only contains the transformer. In 'A' the energy flows through both the transformer and the primary bulk

capacitor. This means that more energy is drawn from the supply and stored in the clamp capacitor, and more energy has to be consequently dissipated during each cycle in order to maintain a stable clamp voltage. For the reason of poor efficiency, this circuit is not often used as a clamp.
However, the circuit does have an alternative use other than as a clamp. If the time constant of RC is made small, then C will discharge during the on time of the MOSFET. At turn off time, current flowing from the transformer is now instantly diverted into the capacitor, and through the series diode. The capacitor can thus slow the rate of drain voltage rise, particularly at higher drain voltage where the non-linear drain capacitance of the MOSFET decreases rapidly. It also provides a commutation path for currents flowing in the primary, so that an abrupt step change in current in the bulk capacitor, supply rail and ground are avoided. This can help to avoid differential noise being created across the supply rail. Both attributes are useful as a preventative measure to reduce EMI at source. This can be lower cost than adding in costly inductive line filters, which can also have a significant impact on efficiency. Slowing the rate of rise in low capacitance transformers also allows more time for the MOSFET to turn off, so the result can be a reduction in dissipation in the MOSFET. Resistor R dissipates the capacitor energy, so no additional power is seen by the MOSFET during turn on. However, the circuit's major disadvantage is that it can be very dissipative in order to achieve any reasonable effect on rise time, and its impact on overall system efficiency must be carefully weighed against the cost of implementing other means of controlling EMI.

Question 2

When designing circuit ‘B’, which of the following are true and which are false?

1、 A transformer with high leakage inductance gives best performance
2、 A tightly controlled drain current limit allows better control of the peak drain voltage
3、 Diode D should be as fast as possible
4、 Decreasing the drain current limit of the device with increasing input voltage will help limit peak voltage
5、 RA should be the lowest value possible
6、 RB should be the lowest value possible
7、 High output loads will create higher peak drain voltages than low output loads
8、 Peak drain voltage should be checked at the worst case conditions of tolerances

Show the Answer

Answer 2

a) A transformer with high leakage inductance gives best performance

FALSE: High leakage is almost always undesirable except in certain specialized resonant topologies.

b) A tightly controlled drain current limit allows better control of the peak drain voltage

TRUE: Controlling the peak drain current limit controls the amount of energy stored in the leakage inductance. This enables better control of the peak energy that must be dissipated in the clamp circuit and therefore more stable performance. Power Integrations devices all feature very tightly tolerance current limits that are 100% tested in production. Moreover, *TOPSwitch®-GX* devices allow the current limit to be set using the X-pin feature, in order to minimize the peak current.

c) Diode D should be as fast as possible

FALSE: The clamp diode characteristics should be carefully chosen for the application (see also PI Power Puzzler #1). In some applications, a slower diode may give a significant improvement in system efficiency, as the turn off current recycles some of the energy stored in the clamp capacitor back into the system. Slower diodes also have the advantage of generating less EMI than a fast diode, and can improve cross regulation. However, while slower diodes can be used when efficiency or EMI is a concern, great care should be taken to check diode temperature under high stress conditions, as diodes slow down as they warm up, and a thermal runaway situation can arise if care is not taken in the selection. A series resistor (RA) should generally be used in conjunction with a slow diode to help control turn off characteristics.

d) Decreasing the drain current limit of the device with increasing input voltage will help limit peak voltage

TRUE: The *TOPSwitch-GX* allows a line dependent current limit to be set using just two resistors, helping to ensure the minimum leakage energy is stored at high line where peak drain voltages are of greatest concern by reducing the

maximum drain current. Without this, under worst-case conditions, significantly higher energy may be transferred to the clamp at high line, which can result in overheating of the clamp, or dangerously high drain voltages.

e) RA should be the lowest value possible

FALSE: RA should be chosen for the highest value that allows the peak drain to remain within the required limits. Making RA low in value will increase the peak diode currents, and speed up turn off time, leading to higher EMI. Conversely, although some energy will be dissipated in RA, a higher value will generally increase the overall efficiency of the supply by decreasing the reset time.

f) RB should be the lowest value possible

FALSE: RB should be chosen for the highest value that allows the peak drain to remain within the required limits. Making RB low in value will decrease the peak drain voltage but will also rapidly lead to increased dissipation in the system, as it will increase the reset time of the leakage inductance current, which in turn diverts energy from the transformer primary for a longer period.

g) High output loads will create higher peak drain voltages than low output loads

TRUE: In *TOPSwitch-GX*, which is a voltage mode, PWM controlled device, for a given transformer design, higher output loads will result in higher peak currents, which in turn will lead to more energy being transferred to the clamping system, and hence higher average voltages. In *TinySwitch®-II* devices, which use fixed current limit, ON/OFF regulated controllers, the effect is not so pronounced. However, when running at high load, less cycles are skipped, so the average voltage on the clamp capacitor will still rise with increased load.

h) Peak drain voltage should be checked at the worst-case conditions of tolerances

TRUE: Worst case combinations of component tolerances, load (both static and transient), temperature and supply rails should be applied and the device carefully monitored to ensure the drain voltage remains within a safe margin of its rated limits.

Question 3

When designing a clamp circuit to ensure the drain voltage remains within safe limits of the device ratings, what are the key points to consider, and what testing would you perform to validate your design?

Show the Answer

Answer 3

The starting point for any clamp design is to determine the maximum allowable voltage of the drain of the MOSFET. Power Integrations devices are 100% tested in production to ensure they meet the datasheet rating for BV_{DSS} of 700 V. In addition, it is prudent to use a safety margin of 5-10% to allow for surge and external AC supply aberrations: consequently, a worse case maximum drain voltage of 650 V is often used as the worst-case design target for a typical power supply.

As the clamp voltage is additive to the input supply rail, the expected limits of supply voltage should also be taken into account. While supplies are usually rated for nominal voltage ranges, surge or swell condition occur in certain markets (i.e. where a nominal 230 VAC input voltages can exceed 300 VAC). This should be taken into account and the worst-case AC input should be used during testing to ensure the BV_{DSS} rating of 700 V is never exceeded. Note that the L pin of the *TOPSwitch-GX* allows an ‘over voltage’ (OV) function to be simply implemented using a single resistor, and can prevent high input voltages from generating high peak drain voltages by shutting off the IC temporarily until the supply drops within acceptable limits. For instance, a 2 M ohm resistor between the L pin and the DC supply will shut down the *TOPSwitch-GX* when the supply exceeds 450 V. Due to its hysteretic behavior, it will only allow the supply to restart when the supply drops below 434 V. These levels can be adjusted by simply changing the value of the resistor. This allows for much better protection that relying purely upon MOV surge suppression devices at the AC input, which have very limited energy capability.

A factor in the amount of energy that the clamp system has to dissipate is the amount of energy stored in the leakage inductance during each cycle. The energy in the leakage inductance, E, is defined by

$$E_{AVE} = \frac{L_{P(LEAK)} I^2_{DRAIN-P(LEAK)}}{2}$$

Where:
L_L is the leakage inductance
$I_{DIODE-P}$ is the peak clamp diode current during clamping.
And $_{(MAX)}$ indicates the worst-case condition of these variables
As a consequence, testing of the supply for peak drain voltage margin should use a transformer at the high end of its leakage inductance specification, $L_{L(MAX)}$.
Note also that the peak diode current, $I_{DIODE-P(MAX)}$, is not necessarily identical to the peak current in the primary. It is typically anywhere from 50%-80% of the peak primary current, and should be measured in the system to verify this. The reason for the difference is due to:

- the effect of the parasitic and / or reflected secondary snubber network capacitance across the primary winding delaying the rise in voltage across the primary inductance
- the effect of the series resistor RA in slowing the rise of the clamp diode current to its maximum value, hence allowing more time for the leakage inductance flux to reset.

Because secondary snubber networks can influence the amount of energy in the clamp system, these components should be carefully chosen to help reduce the peak clamp diode current, and thus lower the peak drain voltage.
As the peak clamp diode current is directly related to the peak primary current, conditions that maximize the primary current should be tested, such as pulsed loads that cause the device to operate at its current limit. Variation in current limit with component tolerances will directly affect the peak drain current. All Power Integrations devices are tested in production for very tight current limit specifications in order to minimize the impact of this. For example, the *TinySwitch-II* devices are 100% tested to a +/-7% limit for peak drain current tolerance.
The resistor RA is effectively in series with the clamp diode, so its value directly affects the peak clamping voltage.
The power dissipated by the clamp resistor RB equals the energy stored each cycle in the clamp capacitor. Thus a resistor at the high end of its tolerance requires a higher voltage across it to dissipate the same amount of energy, which in turn also increases the peak drain voltage. Therefore, measurements of peak voltage should be made using both components at the high end of their tolerance (typically 5%).
As the peak diode current is influenced by the storage time of the diode, measurements should be taken when the energy recovered through reverse turn off currents is at its lowest. This is typically when the diode is operating at the low end of the temperature range, where storage times are typically shortest.
Another parameter that has a direct affect upon the peak voltage is the reflected primary voltage, V_{OR}. This is mostly influenced by the tolerances in the feedback circuit. For testing, the regulated secondary output should be set at the upper end of its tolerance by temporarily adjusting the feedback components, resulting in the maximum value of V_{OR}.

Puzzler 6

Test your power supply design knowledge as it pertains to Power over Ethernet by trying your hand at answering the three questions below.
To learn more about **Power over Ethernet**, visit our PoE page.
The schematic below shows a typical Flyback PoE power supply built with a *DPA-Switch*® power conversion IC and a discrete PoE interface circuit for detection and Class 0 classification per IEEE 802.3af. Limiting the maximum drain voltage that your power switch sees is essential to ensure its reliable operation.

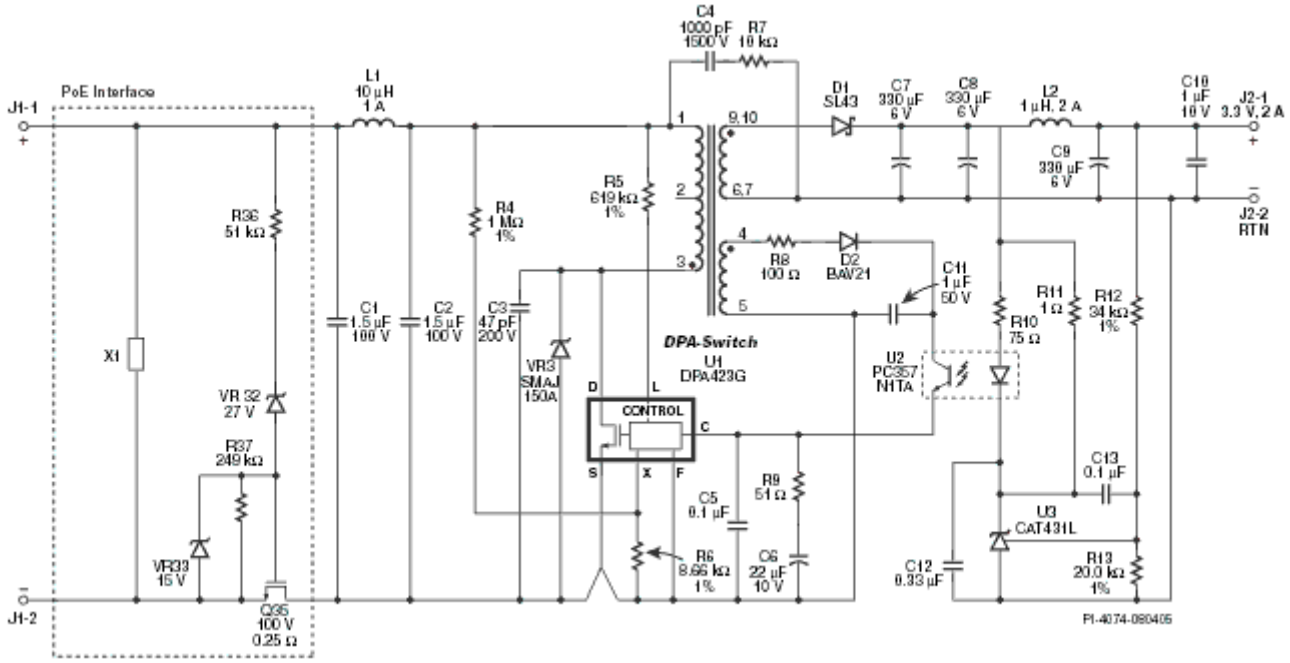


Figure 1 – PoE Class 0 DC-DC Converter using DPA423G.

Question 1

The PD (Powered Device) detection specification requires the PD to present an impedance of between 19 kΩ and 26.5 kΩ at input voltages between 2 VDC and 10 VDC. The classification stage (Class 0) requires the PD to draw a current of up to 4 mA at input voltages of between 14.5 VDC and 20 VDC. Is it possible to implement Class 0 detection and classification features of a PD using a single **passive** component (X1)? What is this component and component value?

Show the Answer

Answer 1

Class 0 detection and classification can be implemented with a single resistor (X1 = 24.9 kΩ), shown in Figure 1.

Class 0 solution:

Detection: Figure 2(a) shows the V-I curve for the detection input voltage range (2.5 VDC to 10 VDC). Resistors in the range of 19 kΩ to 26.5 kΩ would meet this requirement. A resistor value (of 24.9 kΩ) is chosen at the high-end of the admissible range to reduce power dissipation.

Classification: Figure 2(b) shows the V-I curve for the classification input voltage range (14.5 VDC to 20 VDC). Fortunately, Class 0 currents (between 0 mA and 4 mA) can be met with the same 24.9 kΩ resistor used for detection (consuming 0.582 mA at 14.5 VDC and 0.803 mA at 20 VDC).

For a detailed description see Power Integrations Design Idea DI-70 (resistor R51).

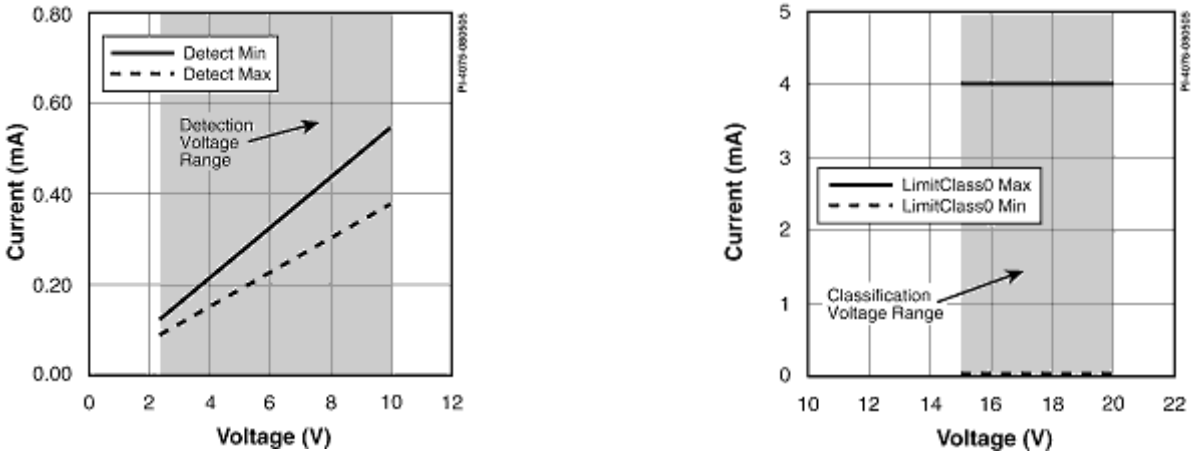


Figure 2 – Class 0 - PoE Detection and Classification Specifications.

Class 1 to Class 3 solution:

Detection: This is exactly the same as for Class 0 above, implemented with a single 24.9 kΩ resistor.

Classification: The solution is a little more complicated than Class 0, but still easily implemented with low cost discrete components (see figure 3). The solution is inexpensive, costing approximately $0.10 to $0.15 in high volumes - much cheaper than a PoE interface IC. Class is programmed with the value of R34 (see table 1). For a detailed description, see Power Integrations Design Idea DI-88.

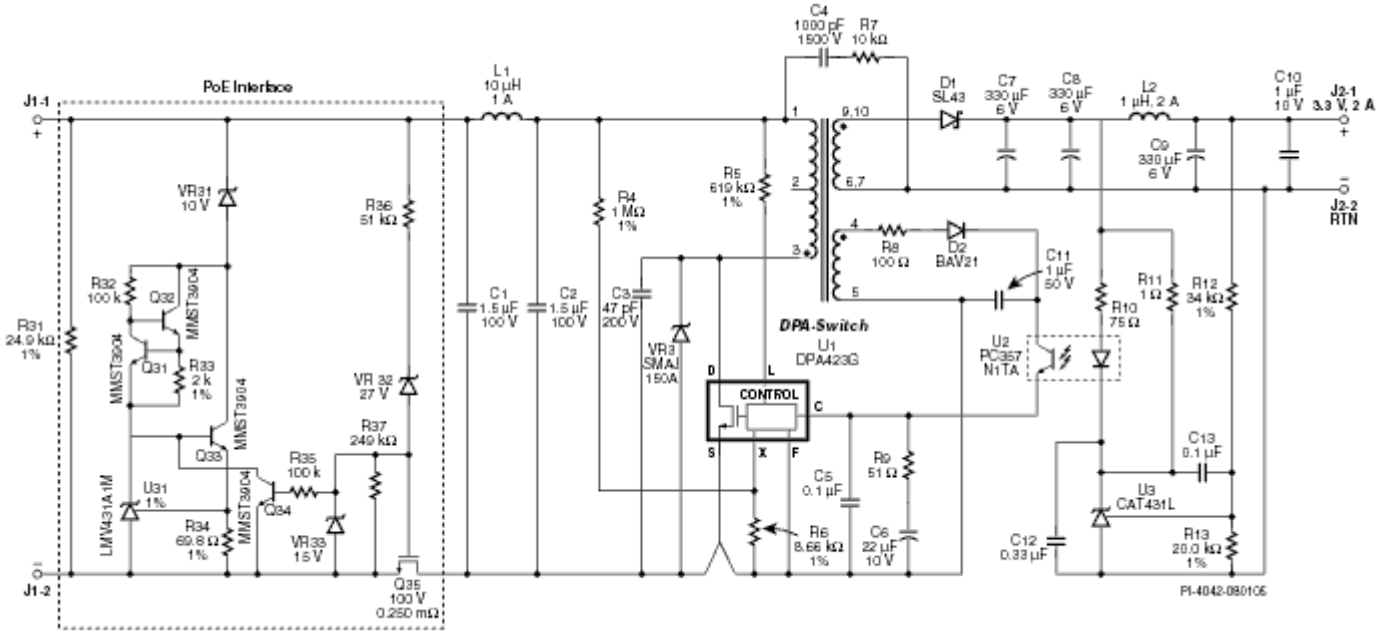
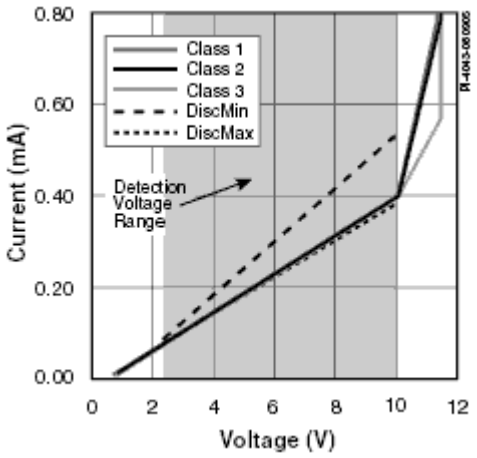


Figure 3 – PoE Class 2 DC-DC Converter Using DPA423G.

Class	P_{OUT} (min.)	P_{OUT} (max.)	I_{CL} (min.)	I_{CL} (max.)	R34
	W	W	mA	mA	Ω
0	0.44	12.95	0.5	4	-
1	0.44	3.84	9	12	133
2	3.84	6.49	17	20	69.8
3	6.49	12.95	26	30	45.3

Table 1 PoE Classification Currents and Power Levels.



(a) Detection Current vs. Input Voltage

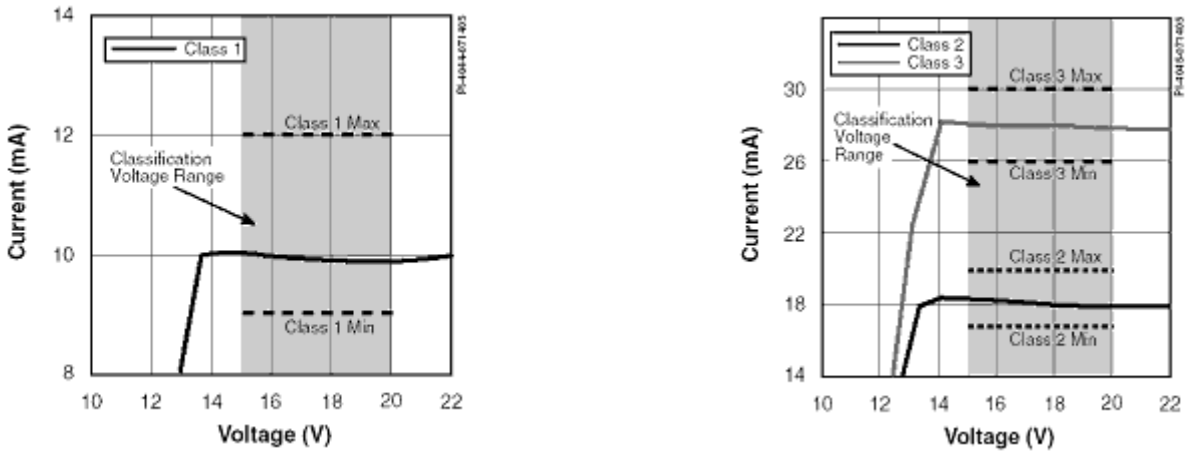


Figure 4 - Class 1 to Class 3 - PoE Detection and Classification Specifications.

Question 2

The PoE standard requires a wide under-voltage lockout hysteresis. The maximum cable impedance from the PSE (Power Sourcing Equipment) to the PD is 20 Ω (up to 100 meters of cable). The PSE output voltage is nominally 44 VDC with a maximum continuous output current of 350 mA. At this current level, what is the voltage at the PD end of the cable? Why is the hysteresis important?

Show the Answer

Answer 2

The answer is the V_{PD_IN} = 37 VDC. If the startup threshold does not include sufficient hysteresis it could cause a power supply to shutdown when drawing maximum load.

$$V_{PD\_IN} = V_{PSE\_OUT} - V_{R\_CABLE}$$

$$V_{R\_CABLE} = I_{LOAD} \cdot R_{CABLE}$$

The CAT-5 cable used for an Ethernet connection can have a resistance of 20 Ω per 100 meters (300 ft). IEEE standards allow CAT-5 (Ethernet) cables to have lengths of up to 100 meters. At startup, the input current to the PD is close to zero. Therefore, there will be almost no drop on the cable. This means that the PD will see the full 44 VDC (min) from the PSE. However, if the PD increases to full power, the input peak operating current of the PD will jump to approximately 350 mA for Class 0 (and Class 3). This in turn will cause an immediate 7 VDC cable drop (350 mA times 20 Ω), reducing the input voltage at the PD from 44 VDC to approximately 37 VDC at the end of the cable.

Description	Min	Max	Unit
PSE Output Voltage	44	57	VDC
PD Input Voltage	37	57	VDC
Difference (V_{PSE} – V_{PD})	7	0	VDC

Table 2 - Output Votlage Range of PSE and Input Voltage Range of PD.

Consequently, the input under-voltage lockout circuit needs to accommodate this 7 VDC operating cable drop. One simple way to implement this is shown below, making use of the under-voltage / over-voltage (UV/OV) functionality of the *DPA-Switch* L pin. The circuit will program the power supply to start when the input voltage exceeds approximately 43 VDC. When the PD begins operating, the under-voltage shutdown threshold will drop back to approximately 33 VDC, thus accommodating the cable drop without shutting down.

Example of wide hysteresis under-voltage lockout

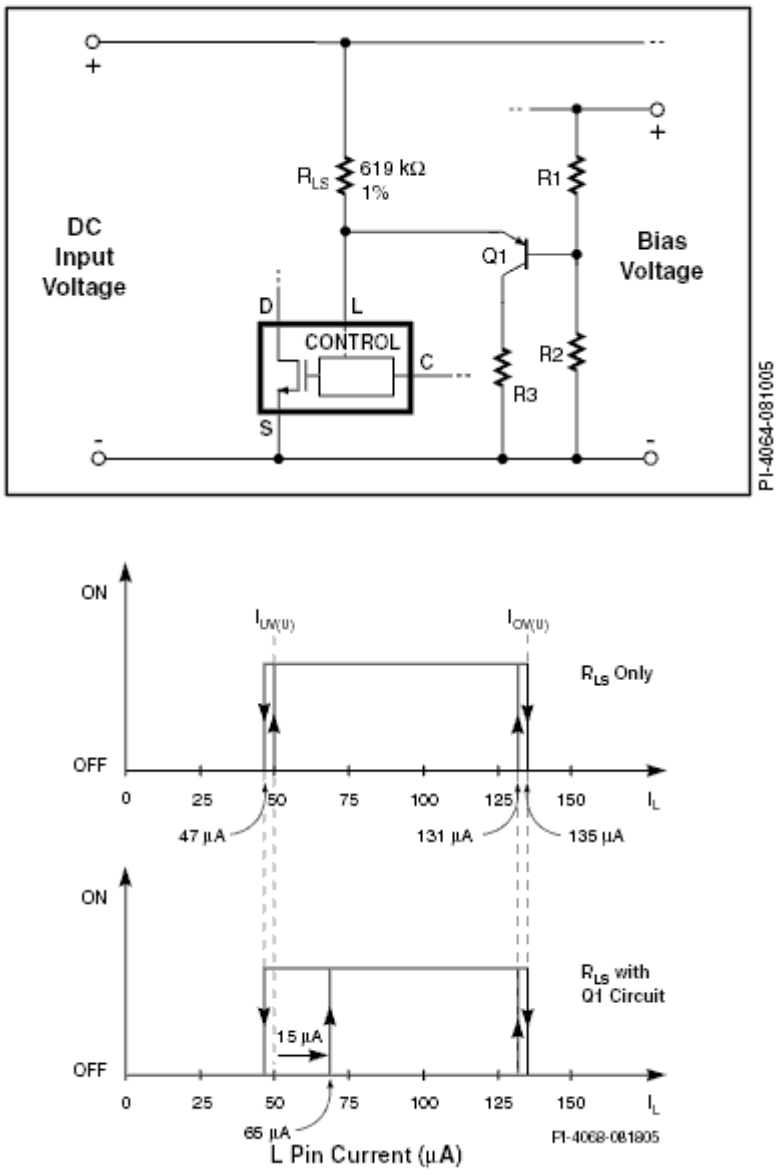


Figure 5 - Circuit for Modified Under-Voltage (UV) Turn-on Threshold with Hysteresis (approximately 10 VDC in this case).

R_{LS} = 619 kΩ		line-sense resistor - sets the default *DPA-Switch* L pin line-sense current
R1 = 10 kΩ		pull-up resistor - turns off Q1 when bias-voltage is active
R2 = 1 MΩ		pull-down resistor - turns on Q1 when bias-voltage is inactive
R3 = 150 kΩ		programs the current drawn from the L pin when Q1 is turned on
Q_1 = 2N3906		pnp-transistor used as a switch to turn on/off R 3 current
Bias Voltage (V_{BIAS}) = 8 VDC		this is an auxiliary supply generated when the *DPA-Switch* is switching

The circuit above allows the under-voltage start-up threshold to be set to approximately 43 VDC and relaxed to approximately 32 VDC once operational. The *DPA-Switch* detects the input voltage via current through resistor R_{LS}. The turn-on threshold is approximately 50 uA above which the *DPA-Switch* is operational. Below approximately 47 uA, the *DPA-Switch* is shut off again. Transistor Q1 is pulled down via resistor R2. This causes a voltage drop across R3 thus subtracting a fixed current (approximately 15 uA) from the L pin as long as Q1 is turned on. When the power supply becomes operational, the bias voltage pulls up via R1, turning off Q1 and thus cutting off the R3 current. Note: due to the L pin synchronization function (with a 1 V threshold), resistor R2 should be sufficiently large to prevent Q1 turn-on below 1 V.

Resistor values R_{LS}, R2 and R3 are calculated as follows:

$$R_{LS} = \frac{V_{UV\_OFF} - V_L}{I_{UV\_OFF}}$$

$$R_3 = \frac{V_L \cdot R_{LS}}{V_{UV\_ON} - I_{UV\_ON} \cdot R_{LS} - V_L}$$

$$R_2 = \frac{\left(V_L - V_{Q1(be)}\right) \cdot R_3 \cdot \beta}{V_L \cdot K} \quad \text{where} \quad \frac{K}{\beta} = \frac{I_b}{I_c} \quad \text{typically choose K = 10}$$

For design verification:

$$V_{UV\_ON} = \left(I_{UV\_ON} + \frac{V_L}{R_3} \right) \cdot R_{LS} + V_L$$

$$V_{UV\_OFF} = I_{UV\_OFF} \cdot R_{LS} + V_L$$

The design target parameters are the following:

V_{UV_ON} = 43 VDC		required input under-voltage threshold for turn-on
V_{UV_OFF} = 31.45 VDC		default input under-voltage threshold for turn-off
R1 = 10 kΩ		this value is assumed as a starting point

From the *DPA-Switch* data sheet we see the following:

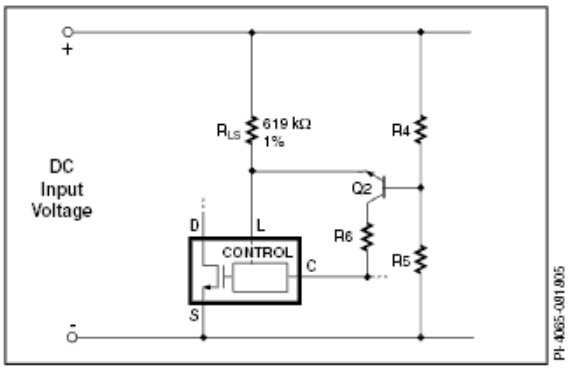
I_{UV_ON} = 50 mA		is the L-pin current at which the device turns on
I_{UV_OFF} = 47 mA		the L-pin current at which the *DPA-Switch* stops switching
V_L = 2.35 VDC		L-pin voltage at I_L=I_{UV_ON}
V_C = 5.8 VDC		Control-pin voltage

And where:

$V_{Q1(be)}$ = 0.7 VDC		transistor base-emitter voltage
b= 100		transistor minimum current gain
K = 10		this is the ratio of transistor bias versus collector current (larger K gives stronger bias)

Example of lowered over-voltage lockout threshold

It is also possible to modify the default over-voltage shutdown threshold to more closely match the 57 VDC maximum input voltage of a PoE system using a similar, but independent network.



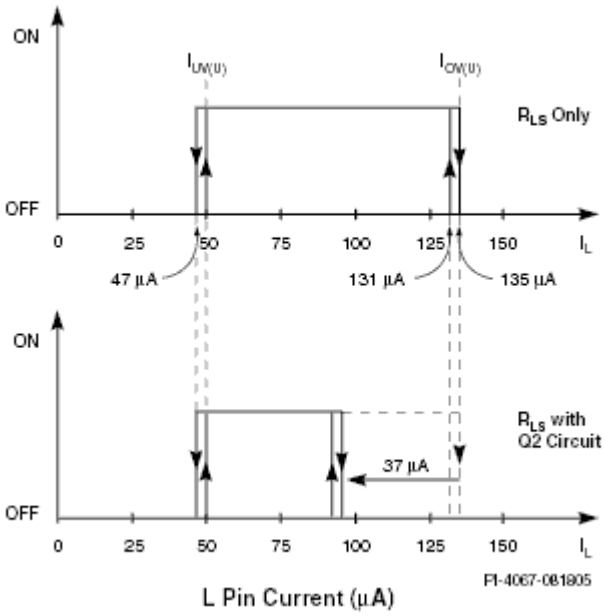


Figure 6 – Circuit For Modified Over-voltage (OV) Threshold.

R_{LS} = 619 kΩ		line-sense resistor - sets the default *DPA-Switch* L pin line-sense current
R4 = 4.7 MΩ		pull-up resistor - turns off Q1 when bias-voltage is active
R5 = 270 kΩ		pull-down resistor - turns on Q1 when bias-voltage is inactive
R6 = 91 kΩ		programs the current drawn from the L pin when Q1 is turned on
Q2 = 2N3904		npn-transistor used as a switch to turn on/off R3 current

The circuit above allows the over-voltage shut-down threshold to be set to approximately 63 VDC (independently of the under-voltage threshold). The *DPA-Switch* detects the input voltage via the L-pin resistor R_{LS}. The turn-off threshold is approximately 135 uA, above which the *DPA-Switch* is turned off. Below approximately 131 uA, the *DPA-Switch* is operational again. At startup, transistor Q2 is pulled off via resistor R5, so as not to interfere with the under-voltage detection threshold. Transistor Q1 is pulled high (on) via resistor R4 and will turn on once the input voltage exceeds the under-voltage turn-on level, at defined threshold voltage ($V_{IN(th)}$ = 60 VDC). Note that the resistor $V_{IN(th)}$ voltage must be above the under-voltage input startup threshold. This connects the Control-pin voltage (V_C) to the L pin via Q2 and R6, thus subtracting a fixed current (approximately 37 uA) from the L pin as long as Q2 is turned on. This subtracted current lowers the over-voltage shutdown input voltage threshold.

Resistor values R4, R5 and R6 are calculated as follows:

$$R_4 \geq \frac{\left(V_{OV\_OFF} - V_L - V_{Q1(be)}\right) \cdot \beta_{min}}{I_{OV\_OFF} \cdot K}$$

$$R_5 \geq \frac{\left(V_L + V_{Q1(be)}\right) \cdot R_4}{V_{OV\_OFF} - V_L - V_{Q1(be)}}$$

$$R_6 = \frac{\left(V_L - V_C\right) \cdot R_{LS}}{V_{OV\_OFF} - I_{OV\_OFF} \cdot R_{LS} - V_L}$$

For verification:

$$V_{IN(th)} = \frac{\left(V_L + V_{Q1(be)}\right) \cdot \left(R_4 + R_5\right)}{R_5}$$

$$V_{OV\_OFF} = \left(I_{OV\_OFF} - \frac{V_C - V_L}{R_6} \right) \cdot R_{LS} + V_L$$

The design target parameters are:

V_{OV_OFF} = 63 VDC		required input voltage threshold for turn-on
$V_{IN(th)}$ = 60 VDC		threshold at which lower-OVLO becomes active
V_L = 2.35 VDC		L-pin voltage at I_L=I_{UV_ON}
V_C = 5.8 VDC		Control-pin voltage

From the *DPA-Switch* data sheet, we see the following:

I_{OV_OFF} = 135 mA		is the L-pin current at which the device turns on
V_L = 2.5 VDC		L-pin voltage at I_L = I_{OV_OFF}
V_C = 5.8 VDC		Control-pin voltage

And where:

$V_{Q1(be)}$ = 0.7 VDC		transistor base-emitter voltage
β = 100		transistor minimum current gain
K = 10		this is the ratio of transistor bias versus collector current (larger K gives stronger bias)

Note2: The D_{MAX} limit of the *DPA-Switch* linearly decreases with increasing input voltage (increasing L-pin current) when using only resistor R_{LS} for under/over-voltage detection. However, when the over-voltage threshold is modified with additional circuitry, this will effectively change the D_{MAX} limit proportionally above the threshold voltage ($V_{IN(th)}$). The power supply designer should therefore make sure that the power supply can still deliver the required power with the reduced maximum duty cycle at high line.

Question 3

The PD inrush current should be less than 450 mA after 1 ms. This allows the input capacitors of the PD to charge during startup, once the PSE output voltage exceeds 30 V. In a particular application, the PSE is connected via a 20 Ω cable to a PD with input capacitance of 3 µF. The PD is turned on as the PSE reaches 30 V. How long will it take for the PD input current to drop below 450 mA? Does the PD meet the PoE requirements? Does the circuit above require any additional inrush limiting components to meet the requirements?

Recalculate the same parameters with an input capacitance of 180 µF. Would any additional inrush current limit circuit be required?

Show the Answer

Answer 3

For 3 µF the charge current to reach 450mA is t = 95 µs.

With this capacitance there is no need for any inrush limiting components on the PD.

The time taken for 99% charge of the input capacitors (C IN) is t = 276 µs.

These two formulae assume that the PD input capacitor starts with zero voltage, and that the output impedance of the PSE is negligible, with an output voltage (V PSE) of 30 V before the input switch is turned on (e.g. Q35 in figure 1):

$$t = -R_{CABLE} \cdot C_{IN} \cdot \ln\left(\frac{i(t) \cdot R_{CABLE}}{V_{PSE}} \right)$$ time taken for current to equal I(t)

$$t = -R_{CABLE} \cdot C_{IN} \cdot \ln\left(1 - \frac{V_{CIN}}{V_{PSE}}\right)$$ time charge time to reach V_{CIN} (C_{IN} < 33 µF)

An input capacitance of approximately 33 µF will take exactly 1 ms for the inrush current to drop to 450 mA. Any larger capacitor will exceed the 1 ms specification.

For instance, the 180 µF capacitance will require a charge time of 5.71 ms to reach 450 mA. It can be seen in this case, the charge period exceeds the 1 ms limit. **However, the PoE specification allows for capacitance up to 180 µF without the need for inrush components on the PD**. For larger input capacitance than this, there is an explicit requirement for the PD to contain inrush-limiting components.

It is possible to use up to 180 µF because during power up, the PSE must limit current to 5 A for the first 1 ms, and then limit the current to 450 mA for the following 50 ms. Thus, even though the charge period exceeds 1 ms to fall below 450 mA, the capacitor charge current will still drop below the required inrush current limit before the 50 ms period. At the end of this period, if the PD consumption still exceeds 450 mA, the PSE disconnects the power to the PD. The current limit is further reduced at this time to the operating continuous current limit (350 mA for Class 0). For designs at this power level the input capacitance normally required would be approximately 5 µF to 10 µF, making it very unlikely that a PD would need on-board inrush current limiting.

Puzzler 7

Take a break from your daily routine and test your power supply design knowledge by trying your hand at answering the three questions below regarding stability of switched mode power supplies.

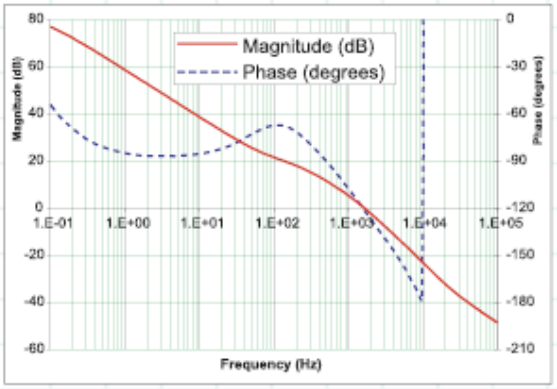


Figure 1A

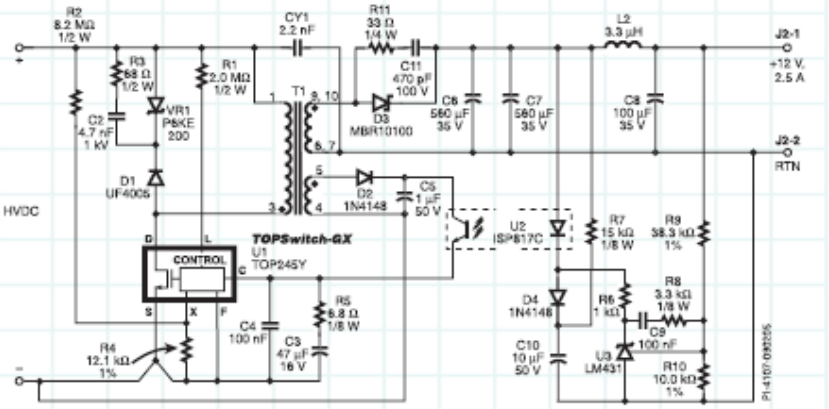


Figure 1B

Question 1

The graph in Figure 1A shows a gain / phase bode plot as measured during the routine development of a switched mode power supply using a *TOPSwitch®-GX* as shown in Figure 1B (See EPR-34 at Design Examples).

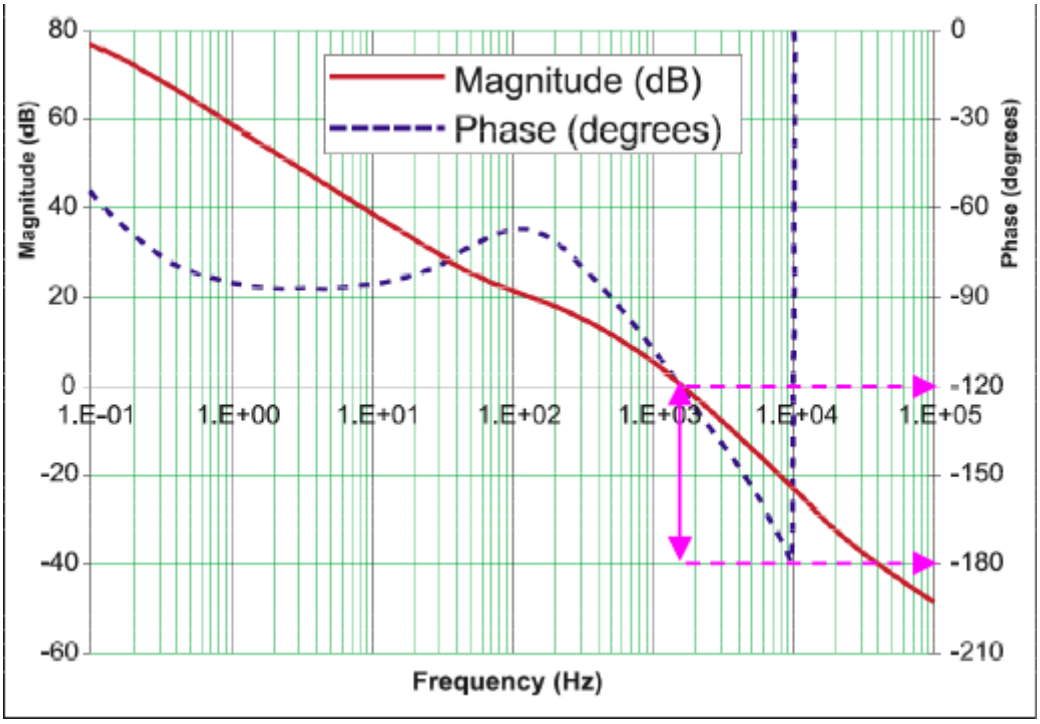
1. Identify the gain crossover frequency and the associated phase margin.
2. How does setting the gain crossover frequency affect the power supply performance?
3. What is the importance of the phase margin?

Show the Answer

Answer 1

a) The plot shows open loop gain and phase measurements of the system. The ‘gain crossover frequency' is the frequency at which the gain is 0 dB (i.e. unity). Oscillation occurs in the system when the open loop gain is unity and the total signal open loop phase shift is zero. Note that the phase measurement in figure 1A is shown excluding the inversion of the summing node, per classical loop theory and in line with common lab measurement apparatus. This definition makes life easier for mathematicians (by making the gain a positive quantity) but requires phase margin definition with respect to 180 degrees. In reality, an additional 180 degrees occurs in the system as a result of the

inversion at the summing node and therefore, the total system phase margin is often shown including the additional 180 degrees. In that case, the phase margin is taken with respect to 360 degrees.
From the graph, the gain crossover frequency is 1.6 kHz and the phase margin is 60 degrees.



b) Crossover frequency generally defines the loop bandwidth and affects the response time to any perturbation to the feedback loop. If this disturbance is faster than the feedback loop response time, the loop cannot respond. This is one reason why there is the urge to push the bandwidth (thus the crossover frequency) higher. However, higher crossover frequency may produce an excessive sensitivity to noise pickup within the loop and one has to be prudent about how much bandwidth is enough. Generally speaking, for offline power supplies a bandwidth of about 1 - 5 kHz is usually sufficient.
c) Phase margin influences the amount of ringing in a power supply. The smaller the phase-margin, the more the ringing. Generally speaking, a phase margin of 45 to 60 degrees is a minimum to guarantee stable loop response over variations in line, load and component tolerances. High phase margin decreases the likelihood that the system (power supply) will go unstable (oscillate). However, high phase margin generally implies lower loop bandwidth, so typically there is an upper ceiling as to how high the phase margin can really be. Generally, increasing phase margin beyond 75 degrees is the point of diminishing return.

Question 2

Waveforms in Figures 2A and 2B show a step load change (top waveform) in two different power supplies, causing the duty cycle to exceed 50%. The output response is shown in the lower waveform.

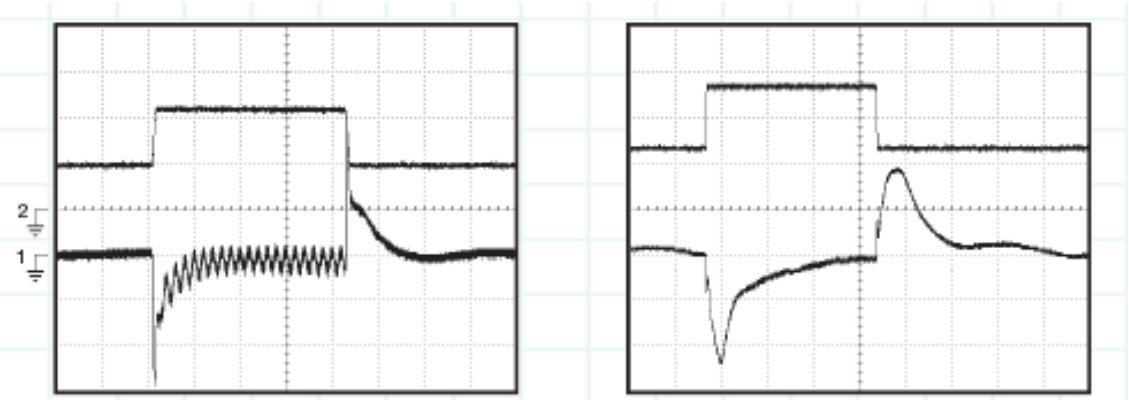


Figure 2A *Figure 2B*

Which supply uses current mode control and which one uses voltage mode control?
What steps need to be taken to avoid the instability shown in Figure 2A?

Show the Answer

Answer 2

Waveform 2A uses current mode control. This evident from the sub-harmonic oscillation once the duty cycle goes beyond 50%, as required for the increased load. This effect is absent in waveform 2B, which uses voltage mode control.

Current mode control needs to employ complicated slope compensation circuits to get around this. Voltage mode control does not need any slope compensation to address duty ratios that may experience wide variation corresponding to a universal input voltage range. Furthermore, voltage mode control is better suited for multiple outputs, making it a good choice for wide input range, multiple output power supplies.

Question 3

When choosing between current mode control and voltage mode control, the designer usually has to consider the relative tradeoffs between each approach and make compromises to achieve the best overall solution.

What are some of the relative pros and cons of current mode control and voltage mode control and why does the *TOPSwitch-GX* provide the best of both worlds?

Show the Answer

Answer 3

Current Mode Pros:

- Inherent line ripple rejection allows low line frequency ripple on output waveform even with moderate gain
- Fast response since the inductor current is used in feedback loop. Does not have to rely on error to first appear on the output before correction action is initiated
- Inherent cycle-by-cycle current limiting
- Gain is independent of line voltage providing similar performance in continuous and discontinuous mode

Current Mode Cons:

- Requires complex slope compensation circuits for stabilizing the loop for duty cycle above 50%
- Requires accurate and reliable current sensing. This usually requires additional components and power loss.
- Accurately sensing the primary current ramp at light loads can be difficult and noise sensitive, adversely affecting signal to noise ratio. In many power supplies (especially at light loads) there is not enough signal to control the power supply.
- Poorer cross regulation (compared to voltage mode) across multiple output supplies

Voltage Mode Pros:

- Single loop so analysis and design is simple.
- No slope compensation required, so therefore can better address wide range input voltages.
- Simple line voltage feed-forward can be used to make ripple rejection comparable to current mode control
- Provides better cross regulation for multiple output supplies

Voltage Mode Cons:

- Line frequency component can be seen on output ripple unless there is a large loop gain or feed-forward.
- Difference in gain while moving from continuous to discontinuous conduction mode means a design cannot be simultaneously designed to have high bandwidth in both modes, which may affect line ripple rejection etc.

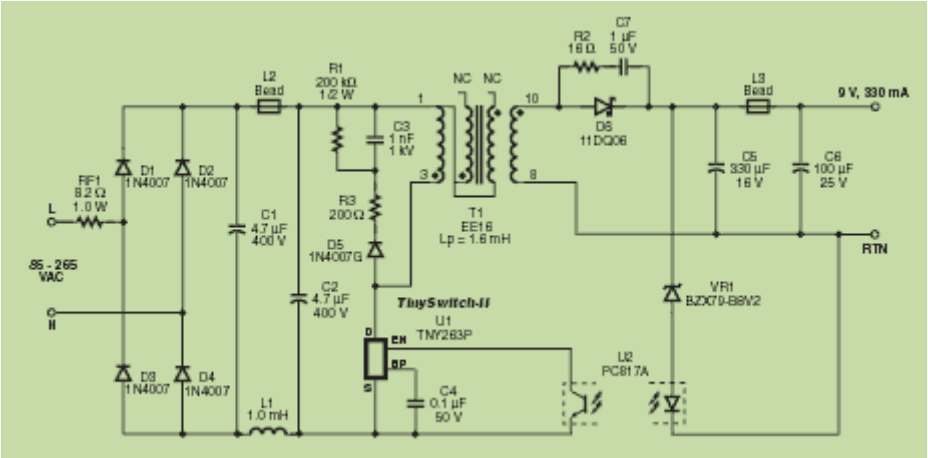
TOPSwitch-GX provides the best of both worlds in many applications because of its highly integrated feature set allows comparable performance to current mode to be achieved with the simpler topology of voltage mode. In addition, the feature set also simplifies the overall design process:

- The L-pin allows feed-forward from the supply rail using a single resistor, simplifying line ripple rejection and providing both overvoltage and undervoltage protection.
- Integrated cycle-by-cycle current limiting and output short circuit protection within the integrated chip.
- Current sensing is achieved by lossless sensing of the primary current, accurately trimmed to tight tolerances, allowing for unbeatable output protection and outstanding system robustness.

- Current sense level can be trimmed by the X-pin to suit individual applications.
- *PI Expert*™, the powerful design software from Power Integrations, simiplifies transformer and system design using *TOPSwitch-GX.*
- The frequency pin (F-pin) allows the choice of operating frequency to best suit your design.

Puzzler 8

Take a break from your daily routine and test your power supply design knowledge by trying your hand at answering the three questions below concerning conducted EMI.



The schematic to the right shows a typical Flyback AC-DC power supply delivering 3 W and utilizing a TNY263P power conversion IC.

Figure 1 - *TinySwitch®-II* 3.0 W Adapter

Question 1

What are the EMI related components in this design? Which are used for differential-mode EMI and which are used for common-mode EMI?

In some designs a y-capacitor is used across the isolation barrier to attenuate common-mode EMI. Safety regulations specify the y-capacitor maximum leakage current at worst case input voltage and frequency.

a. For a maximum leakage current of 0.5 mA at 230 VAC and 50 Hz, what is the maximum y-capacitor value?

b. For some portable devices, the maximum leakage current is 50 µA. At 230 VAC and 50 Hz, what is the maximum y-capacitor value?

Show the Answer

Answer 1

Differential-mode EMI related components

In general applications the following components are used to help reduce differential-mode EMI: Pi-filters, which come in several combinations of resistor, inductor, capacitor, and sometimes ferrite beads. Typically pi-filters are put on the primary side. An X-capacitor is another solution to decouple differential switching noise as well as input diode-generated noise. X-capacitor values above 0.1 µF must have a parallel resistor to ensure that it discharges within a specified period for safety reasons when the input power is disconnected.

In this design: Specifically: L1, L2, C1 and C2 provide differential filtering while the primary clamp (D5, R3, C3 & R1) and output snubber (R2, C7) influence common mode EMI.

Common-mode EMI related components

The Y-capacitor is one of the most frequently used solutions to attenuate common-mode EMI. A common-mode choke either at the input or output is also sometimes used. In some cases, a ferrite bead around the output cable also reduces high frequency common mode EMI but is mostly effective for radiated rather than conducted emissions.

In this design: Specifically in this design, the transformer (T1) shielding reduces common mode EMI.

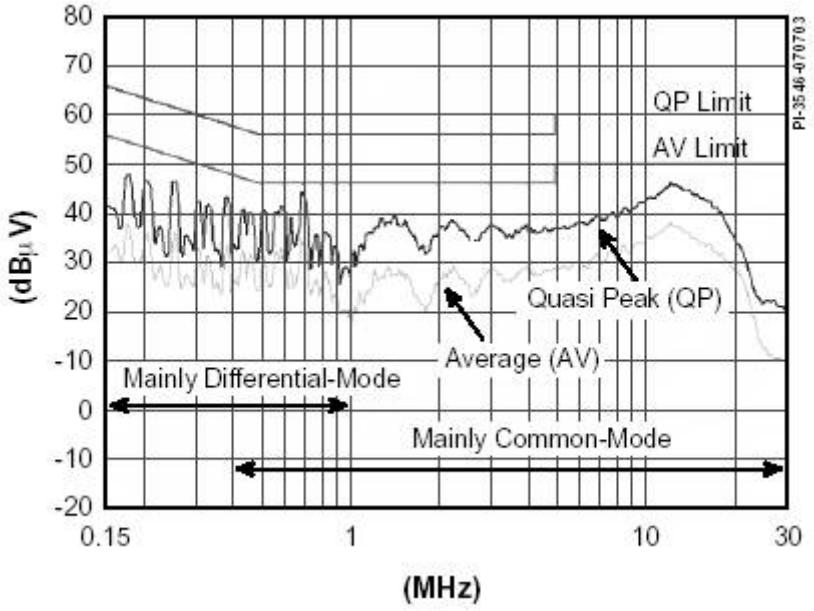


Figure 2 - Portion of Frequency Spectrum showing areas of Differential Mode and Common Mode Noise

Y-capacitor Answers:

In some designs, Y-capacitors are necessary to reduce the common-mode EMI. They work by providing a local shunt path for the displacement currents to flow without leaving the power supply. The value of the Y-capacitor is limited by the permissible earth leakage current allowed. This maximum earth leakage current is governed by standards (IEC60601) and depends on the type of power supply.

$X_c = 1/(2*\pi*f*C)$	- capacitor reactance (impedance)
$I_{leak} = V_{in}/X_c = V_{in}* 2*\pi*f*C$	- earth leakage current
$C = I_{leak}/ (2*V_{in}*\pi*f)$	- capacitor value for given conditions

Using worst-case voltage (i.e. 115 % of V_{in} and 106% of f_{line}), the Y-capacitor value is calculated as follows:

C = 0.5 mA / (2 * 230 *1.15 * 3.1415 * 50 * 1.06)

C = 5.7 nF (for 0.5 mA earth leakage current)

C = 50 mA / (2 * 230 *1.15 * 3.1415 * 50 * 1.06)

C = 567 pF (for 50 mA earth leakage current)

In practice, a standard value of at least 20% less (4.56 nF/454 pF) would be selected to take capacitor tolerance into account.

For power supplies where the output is accessible and not connected to protective earth ground (e.g. mobile phone chargers), the leakage current is limited to 0.25 mA. This limits the maximum Y-capacitor value to 2.2 nF.

Question 2

TinySwitch-II and many of the Power Integrations AC-DC conversion ICs contain a feature called "frequency jitter." This feature varies the switching frequency over a specified range to spread the energy of the switching harmonics over larger frequency bands. The technique is similar to FM modulation, where the jitter repetition (modulation) frequency is 250 Hz, the frequency deviation is ±4 kHz and switching (carrier) frequency is 132 kHz. Without jitter, each harmonic of the switching frequency is a single discrete frequency. However, when jitter is added, each harmonic will spread over a larger band of frequencies. To aid in calculation, we will assume that both switching and jitter signal are sinusoidal. What is the bandwidth of the 5^{th} harmonic when using jitter?

Also, what is the range of overall conducted EMI improvement (in dB) for Quasi-peak (QP) and Average (AV), when using jitter?

Show the Answer

Answer 2

The bandwidth at 5th harmonic will be **40 kHz**.

Frequency jitter results in about **3 to 5 dB** improvement in **Quasi-peak** EMI measurements and **10 to 15 dB** improvement in **Average** EMI measurements.

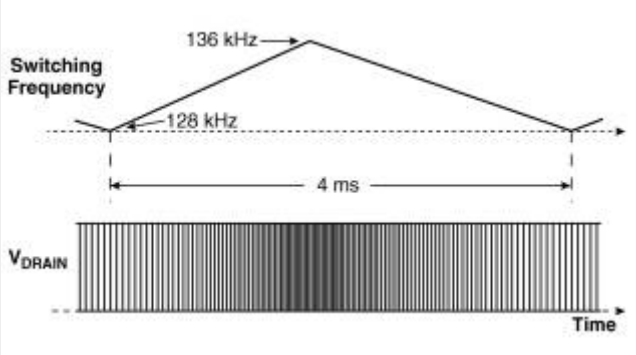


Figure 3 - *TOPSwitch®-GX* Jitter Frequency

PARAMETER	VALUE
Frequency	132 kHz / 66 kHz
Jitter range	±4 kHz / ±2 kHz
Jitter repitition	250 Hz

PI-4223-102705

Figure 4 - *TOPSwitch-GX* Jitter Parameters

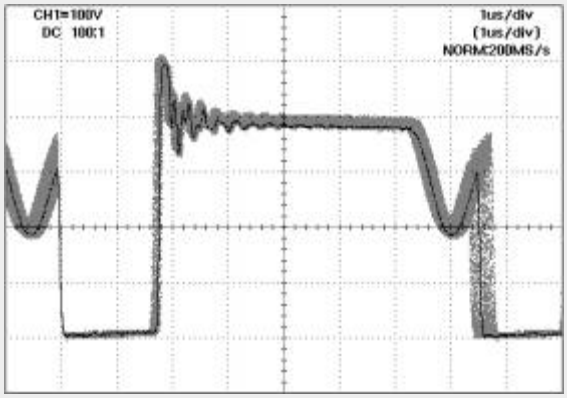


Figure 5 - *TOPSwitch-GX* Jitter Waveform

Theory:

The frequency jitter function is like an FM modulator. The carrier frequency (f_c) is the switching frequency (132 kHz). The frequency deviation (Δf) is defined as "jitter range" of ±4 kHz. The modulation frequency (f_m) is the "jitter repetition" (250 Hz).

The unmodulated carrier waveform is defined as:

$x_c(t) = X_C*cos(2\pi f_C*t)$

The jitter (modulator) waveform is defined as:

$x_m(t) = X_m*cos(2\pi f_m*t)$

The composite FM-modulated waveform then becomes:

$x(t) = X_C*cos[2\pi f_C*t+ \beta*sin(2\pi f_m*t)]$

Where the modulation index (b) is defined as:

$\beta = X_m . \Delta f/f_m$

$\beta = \Delta f/f_m$ *assuming* $X_m = 1$

And where the instantaneous frequency of the composite signal is:

$f = f_C*[1+ (\Delta f/f_c)*cos(2\pi f_m*t)])$

Carson's rule gives a good approximation of the bandwidth containing 98 % of the power of each harmonic:

$B_{nT} = 2* \Delta f*(n*\beta +1)/\beta$	where n is the number of the harmonic (n=1 for fundamental, n=3 for 3rd,etc)

A wideband FM system is one where β is very large (β>> 1), the bandwidth of each harmonic is approximated by:

$B_{nT} = 2* \Delta f*n$	where n is the number of the harmonic (n=1 for fundamental, n=3 for 3rd,etc)

Example:

The frequency deviation and modulation frequency are:

Δf = 4 kHz

f_m *= 250 Hz*

If we consider the fundamental frequency of the switching waveform, then we will have the following (n = 1) :

F_{c1} = 132 kHz	center frequency of fundamental
β = 4 kHz / 250 Hz = 16	modulation index
B_{1T}= 2 * 4 kHz * (1* 16 +1)/16 = **8.5 kHz**	bandwidth at fundamental

Let's consider the 5th harmonic (n = 5)

F_{c5} = 5 * 132 kHz = 660 kHz	center frequency of 5th harmonic
β = 4 kHz / 250 Hz = 16	modulation index
B_{5T}= 2 * 4 kHz * (5* 16 +1)/16 = **40.5 kHz**	bandwidth 5th harmonic

Explanation:

It can be seen that for the fundamental harmonic (n=1), the bandwidth (BW) without jitter would be theoretically zero, but when jitter is added, this bandwidth increases to approximately 8.5 kHz. At the 5th harmonic (n = 5), the bandwidth increases from near zero to approximately 40.5 kHz. At higher harmonics, the bandwidth is spread over a progressively larger frequency deviation.

Conducted EMI receivers have "frequency bins" of 9 kHz in bandwidth. If all the energy of a particular harmonic falls entirely within one frequency bin, then the EMI receiver will register 100 % of that harmonic magnitude at a given single spot frequency. However when frequency jitter is added, the energy of a single harmonic is spread over a wider frequency range (8.5 kHz for the fundamental but wider frequency range for higher harmonics). As a result, the magnitude registered by the EMI receiver will be approximately divided by the number of frequency bins over which the energy is spread. If the energy is spread over at least 2 bins, then the magnitude is reduced by a factor of 50% or at least 3dB.

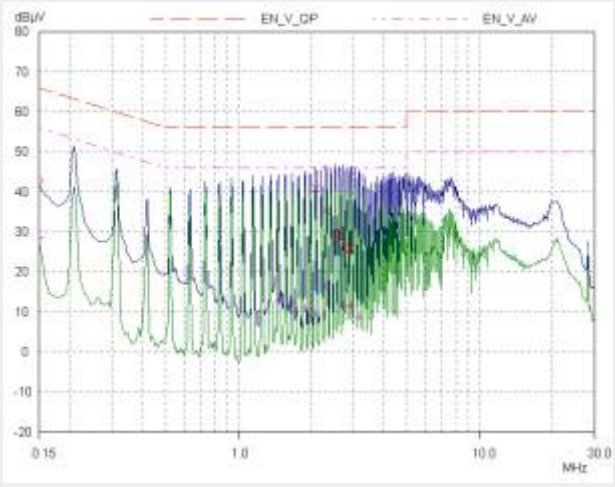


Figure 6 - *TOPSwitch* (100 kHz without jitter) Conducted EMI versus Frequency
Blue: Quasi-Peak (QP)
Green: Average (AV)

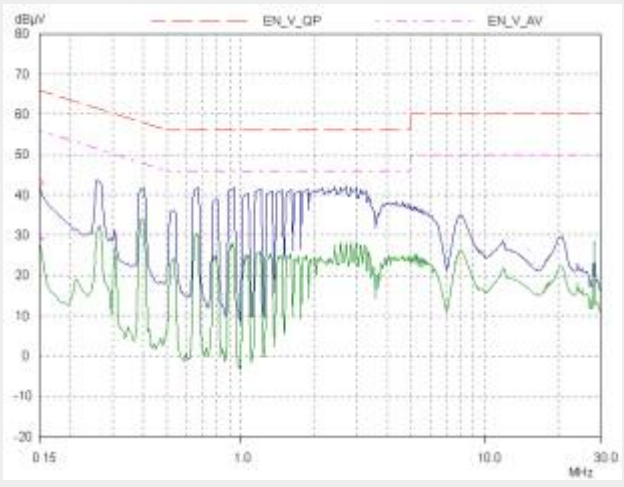


Figure 7 - *TOPSwitch-GX* (132 kHz) with jitter Conducted EMI versus Frequency
Blue: Quasi-Peak (QP)
Green: Average (AV)

The plot on the left shows the conducted EMI for a *TOPSwitch-II* TOP224 power supply switching at 100 kHz without jitter. The plot on the right shows conducted EMI for a *TOPSwitch-GX* TOP244 power supply switching at 132 kHz with jitter. The same board and same load currents were used for both measurements. Without jitter, the switching harmonic peaks are discrete and narrow. With jitter, the switching harmonic peaks are lowered and smoothed. Higher harmonics are smoothed into a more continuous response.

In reality, the switching waveform contains many complicated harmonics and the jitter modulation is a triangular waveform (not sinusoidal). Therefore, the results of jitter will not exactly match formulaic approximations. However, empirical data shows that jitter gives 3 to 5 dB improvement in quasi-peak EMI and 10 to 15 dB improvement in average EMI measurements.

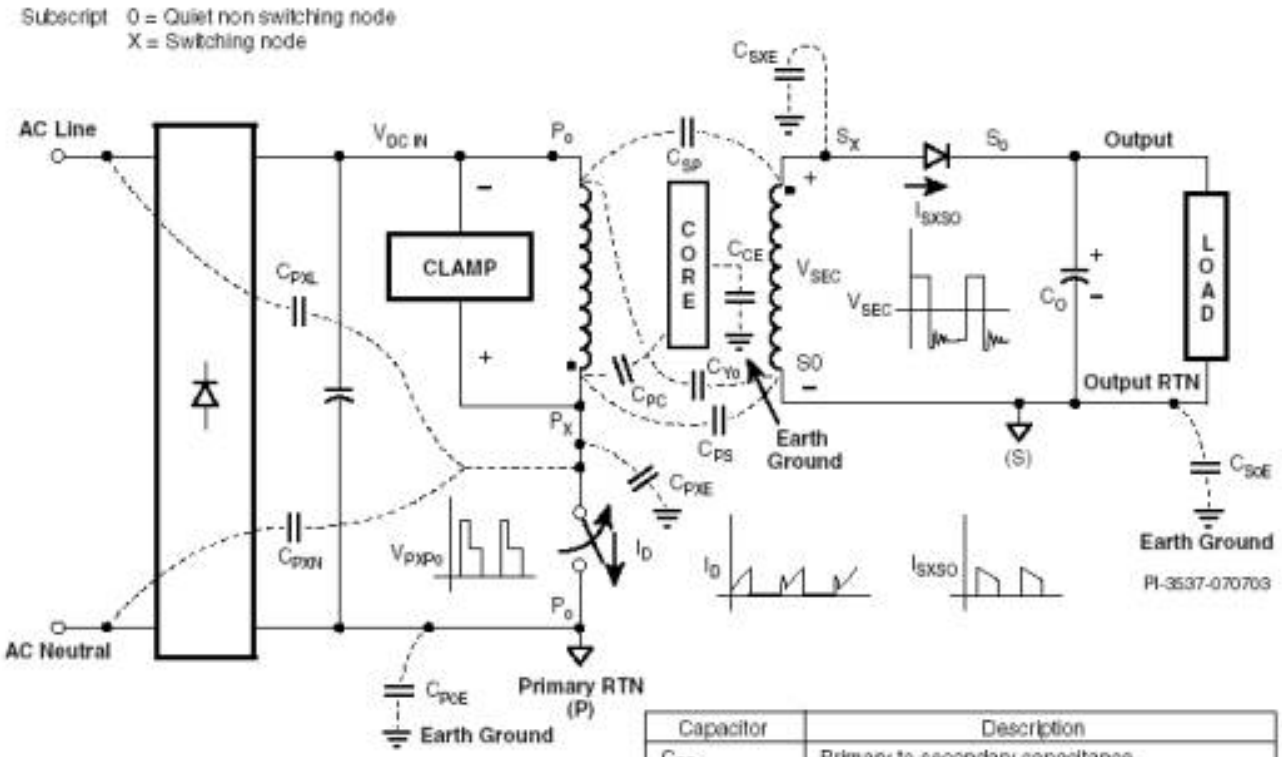
Question 3

On transformer (T1) in the schematic above there are unterminated transformer windings (designated with an NC "no-connection" symbol). What is their function and how do they help reduce EMI?

Show the Answer

Answer 3

Common-mode EMI occurs when the switching signal of the power supply is coupled to earth ground through parasitic capacitances and observed at the inputs of the primary of the power supply (via EMI detection equipment). When this loop is completed, these displacement currents will register as common-mode EMI. Figure 8 shows some of the parasitic capacitances, which facilitate this electro-static coupling between switching (noisy) nodes and earth ground.



Capacitor	Description
C_{PS}	Primary to secondary capacitance
C_{SP}	Secondary to primary capacitance
C_{PC}	Primary to transformer core capacitance
C_{CE}	Transformer core to earth ground capacitance
C_{Y0}	Capacitance across "quiet" nodes of transformer
C_{PXL}	Capacitance between switch and AC line
C_{PXN}	Capacitance between switch and AC neutral
C_{S0E}	Output RTN to earth ground
C_{P0E}	Primary RTN to earth ground
C_{PXE}	Primary switching node to earth ground
C_{SXE}	Secondary switching node to earth ground

Figure 8 - EMI Sources and Coupling

The unterminated windings on the transformer schematic act as electro-static shields within the transformer. The transformer shields do two things: first, they actively cancel some of the switching signals, significantly attenuating the composite signal across the parasitic capacitance and secondly, the shields also significantly reduce all major transformer parasitic (capacitive) coupling paths. Both of these features allow the transformer shielding to significantly attenuate common-mode EMI. In some cases, this is to such an extent as to allow removal of the Y-capacitor.

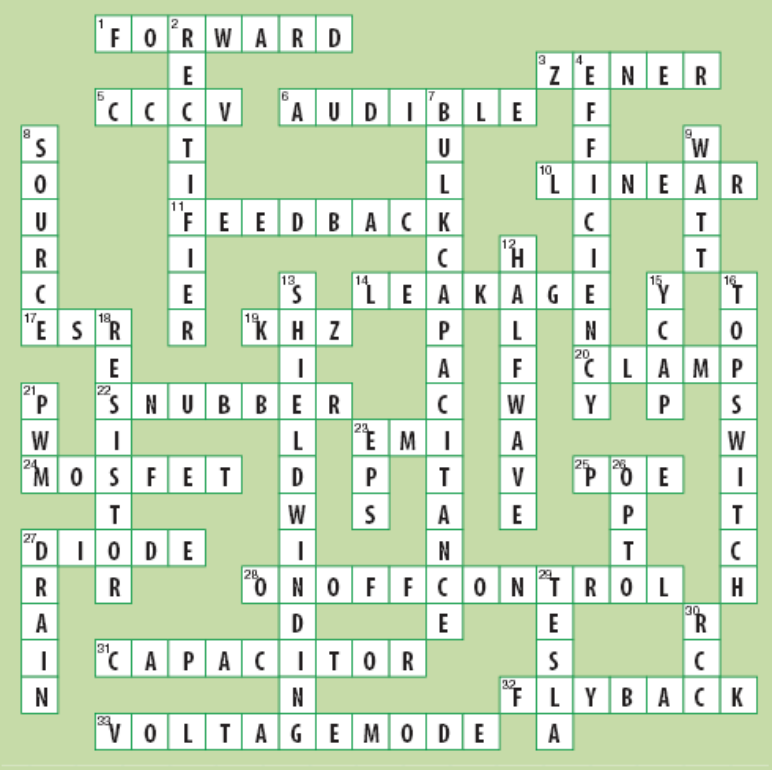
PI Expert™ Suite is a design tool available free of charge from Power Integrations which includes the calculations for transformer shielding construction. The program guides and automates the entire power supply design process. The software allows even less experienced designers to complete a transformer design that will pass conducted EMI, in most cases without the need for a Y-capacitor.

Puzzler 9

Take a break from your daily routine and test your power supply design knowledge by trying your hand at the crossword puzzle below.

ACROSS

1. Topology for high current
2. Two terminal regulator
3. Charger profile
4. Noise, but you can't LISN for it
5. AC-DC conversion technology, not efficient
6. Information from the front
7. Inductance, not coupled
8. Dissipative capacitor parasitic
9. 1000s inverted time
10. Limits voltage spike after switching
11. Secondary source of supression
12. Unwanted, but best not allowed to leave
13. Specified by $R_{DS(ON)}$
14. 802.3af
15. PN, connected
16. *TinySwitch*® operating principle
17. Blocks DC
18. Efficient and simple SMPS topology
19. The best control scheme for multiple output designs



DOWN

1. Turns AC to DC
2. What the doe's star seeks
3. Power reservoir
4. Ground for the low side

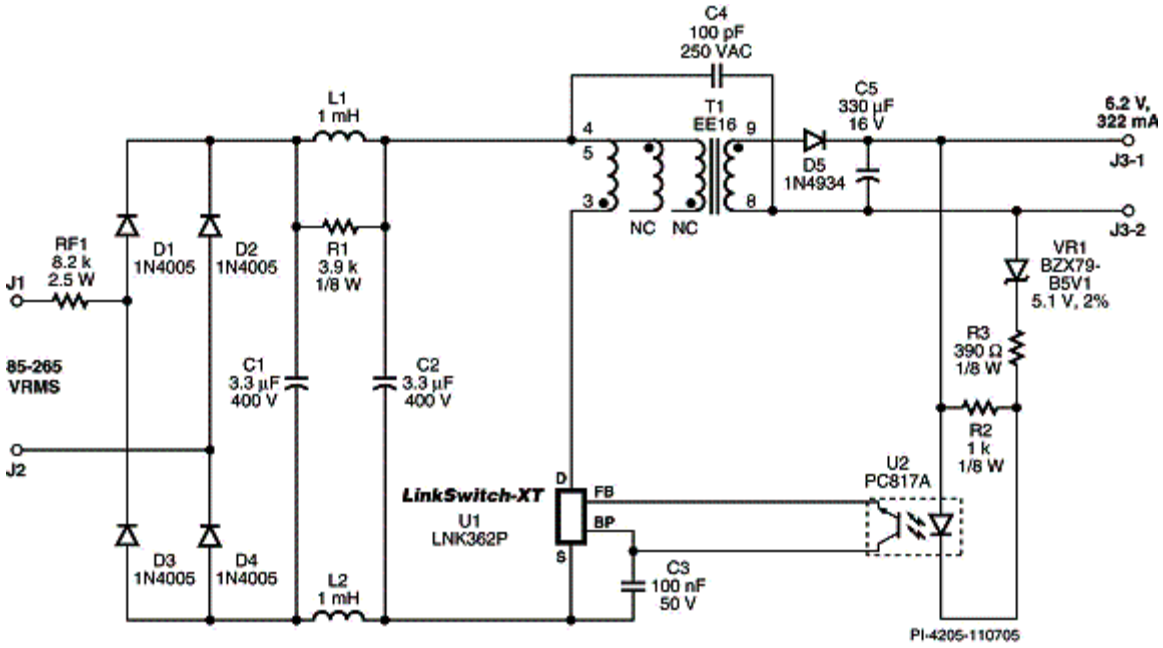
5. A powerful Scottish gentleman
6. A 50% enthusiastic goodbye
7. Reduces electrostatic coupling in transformers
8. An AC path from primary to secondary

1. The original high-voltage integrated switcher IC
2. _____ values sum in series
3. A Top regulation method
4. External Power Supply
5. Communicates with itself at a required distance
6. Electron sink
7. Nikola's magnetic flux
8. Converter type with high switching frequency at no load

Puzzler 10

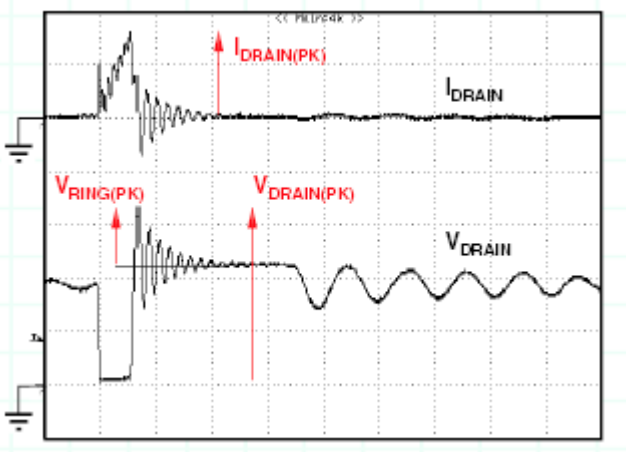
Take a break from your daily routine and test your power supply design knowledge by trying your hand at answering the three questions below regarding a novel flyback power supply design that doesn't require the usual RCD clamp network . Then check your answers and enter for a chance to win a new Apple iPod Nano.

The schematic below shows a simple adapter power supply using a *LinkSwitch-XT* power conversion IC. Part of the simplicity of this design is the absence of the clamp components normally needed to limit the peak drain voltage.



Question 1

Which of the following correctly identifies the major circuit parameters that determine the peak ring voltage ($V_{RING(PK)}$)?



Drain Voltage and Current (200 V, 100 mA, 2 µs/div.)

a. Primary inductance, drain capacitance and input voltage
b. Leakage inductance, input voltage and peak drain current
c. Leakage inductance, transformer turns ratio, output voltage, input voltage and peak drain current
d. Leakage inductance, drain capacitance and peak drain current

Show the Answer

Answer 1

The answer is d. The ring shown is caused by the leakage inductance. The peak-peak ring voltage is a function of drain current, primary node capacitance and leakage inductance. This ring sits on top of the sum of the DC input voltage (V_{DC}) and V_{OR}, the reflected output voltage
$[(V_{OUT} + V_F) \times (N_P/N_S)]$

Question 2

If the drain current at the end of the on-time (**I_DRAIN(PK)**) is doubled, the peak ring voltage will:

a. Not change
b. Double
c. Halve
d. Quadruple

Show the Answer

Answer 2

The answer is b. The voltage is derived by conservation of energy. The energy stored in the leakage inductance at peak drain current is equal to the energy stored in the drain node capacitance at peak drain voltage.

$$\frac{1}{2} \cdot L_{LK} \cdot I_{D(PK)}{}^2 = \frac{1}{2} \cdot C_D \cdot V_{D(PK)}{}^2$$

Solving for $V_{D(PK)}$,

$$V_{D(PK)} = \sqrt{\frac{L_{LK} \cdot I_{D(PK)}{}^2}{C_D}}$$

If $I_{D(PK)}$ doubles, then $V_{D(PK)}$ doubles. This limits the practical maximum drain current in designs where the primary capacitance (the majority of the drain node capacitance) is relied upon for clamping.

Question 3

Which equation below is used to determine the peak drain voltage (**$V_{DRAIN(PK)}$**) in a *Clampless* design?

a. $V_{DRAIN(PK)} = V_{DC} + (V_{OUT} + V_F) \times (N_P/N_S) + (I_D\ 2 \times L_{LK}/C_D)^{1/2}$
b. $V_{DRAIN(PK)} = V_{DC} + (I_D\ 2 \times L_{LK}/C_D)^{1/2}$
c. $V_{DRAIN(PK)} = V_{DC} + (V_{OUT} + V_F) \times N_P/N_S$

What method can be used to estimate the drain node capacitance using the value of the primary inductance and the drain voltage waveform?

V_{DC} is the DC voltage across the bulk capacitor C2.
V_{OUT} is the DC output voltage.
V_F is the output rectifier's forward voltage drop.
N_P is the primary's number of turns.
N_S is the secondary's number of turns.
I_D is the peak drain current at the end of the on cycle.

L_{LK} is the leakage inductance.
C_D is the drain node capacitance.

Show the Answer

Answer 3

The answer to the first part is (a). The peak drain voltage is the sum of three terms.

- The DC input voltage (V_{DC})
- The reflected output voltage, V_{OR}, (V_{OUT} + V_F) x (N_P/N_S)
- The peak ring voltage $(I_D^2 \times L_{LK}/C_D)^{1/2}$

For practical designs this limits the maximum allowable drain current to approximately 150 mA, which is where the current limit for PI products (*LinkSwitch-LP* and *LinkSwitch-XT*) designed for use in Clampless design is set and very tightly toleranced (±7%).

In a given design all the variables except the drain node capacitance (C_D) are fixed making controlling the value of C_D important. However the majority of this value is determined by the transformer winding capacitance allowing this to be controlled by specifying the maximum allowable transformer resonant frequency. In practice there is little variation as there is little mechanical variation of the windings.

The answer to the second part is the relaxation ring.

The relaxation ring occurs when the energy stored in the transformer is zero and the output diode has stopped conducting. This lower frequency ringing (than the leakage inductance ring) is a function of primary inductance and drain node capacitance. As the primary inductance is usually known and the relaxation ring frequency can be measured the capacitance can be estimated using the expression:

$$f = \frac{1}{2\pi\sqrt{L_P C_D}}$$

Solving for C_D,

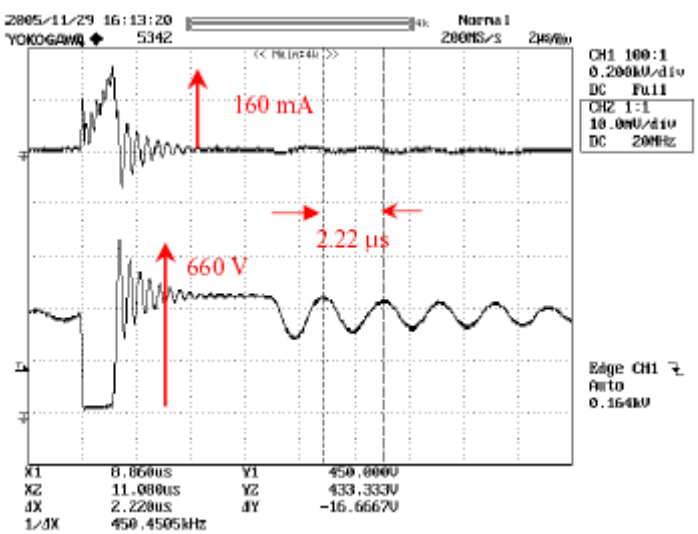
$$C_D = \frac{\left(\frac{1}{2\pi f}\right)^2}{L_P}$$

As an example the waveform below was captured from a LNK362 power supply with a primary inductance of 2.6 mH. The relaxation ring frequency was measured as 450 kHz. Therefore the total drain node capacitance can be estimated as:

$$C_D = \frac{\left(\frac{1}{2\pi \times 450 \times 10^3}\right)^2}{2.6 \times 10^{-3}} \quad = 48\text{pF}$$

The resonant frequency of the transformer itself was measured at 549 kHz giving a transformer capacitance of 32 pF (using the same expression). The difference (16 pF) can be attributed to the MOSFET capacitance, which is also well controlled.

Using the expression for the peak drain voltage we can estimate what the voltage for this design would be based on the measured drain node capacitance and peak drain current at highest line voltage of 265 VAC (375 VDC):



Drain Voltage and Current (200 V, 100 mA, 2 µs/div.)

$$V_{DRAIN(PK)} = V_{DC} + V_{OR} + \sqrt{\frac{L_{LK} \cdot I_D^{\,2}}{C_D}}$$
$$= 375 + 80 + \sqrt{\frac{77\times10^{-6} \cdot (160\times10^{-3})^2}{48\times10^{-12}}}$$
$$= 657\ \text{V}$$

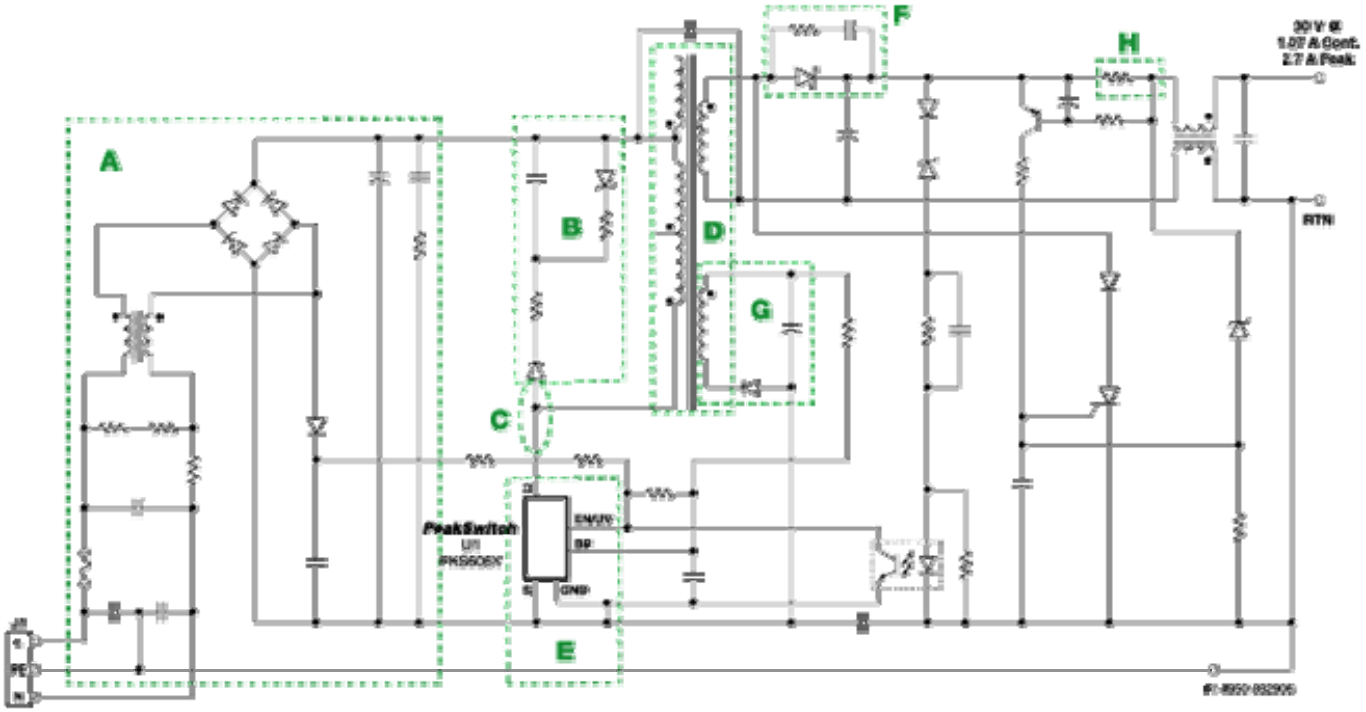
The actual measured voltage was 660 V giving adequate margin to the 700 V MOSFET BV_{DSS} rating.

Puzzler 11

Test your power supply design knowledge as it pertains to power delivery by trying your hand at answering the three questions below. Then check your answers and enter for a chance to win a new Apple iPod nano. The schematic below shows a 32 W average (81 W peak) Flyback power supply using a PeakSwitch™ power conversion IC. In a Flyback converter, output power can be expressed as follows:

$$P_O = \frac{1}{2} \cdot L \cdot (I_{PK}^2 - I_{INIT}^2) \cdot f \cdot \frac{\eta}{Z \cdot (1-\eta) + \eta}$$

where L is the primary inductance, I_{INIT} is the initial and I_{PK} is the final primary current value for each switching cycle, f is the switching frequency, and h is the efficiency. The loss allocation factor (Z) indicates the proportion of losses between primary and secondary and is defined as secondary-side losses divided by the total losses of the supply (0 ≤ Z ≤ 1). A value of 1 indicates that all losses are on the secondary-side of the power supply while a value of 0 indicates all the losses are on the primary-side.



A. Input Stage:____	**B.** Clamp:____	**C.** Drain Node Capacitance:____	**D.** Core Loss:____ , Winding Loss:____
F. Rectifer and Snubber:____	**G.** Bias Supply:____	**H.** Current Sense:____	**E.** Switching Loss:____, Conduction Loss:____

Question 1

If the primary winding copper losses are increased by 100 mW and the secondary winding copper losses decreased by 100 mW.

a. What is the effect on the Z factor?

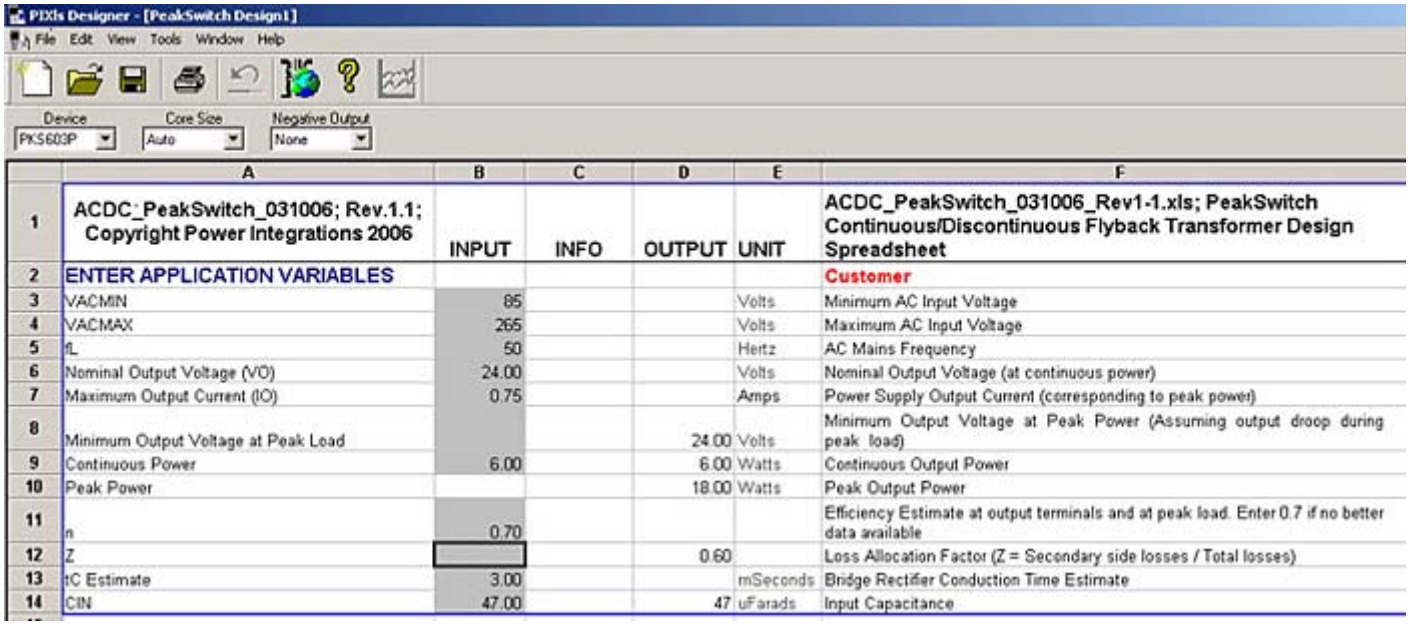
b. What is the effect on the primary inductance value?

Show the Answer

Answer 1

a) As the secondary-side losses have decreasted and total losses have remained the same, by definition Z has decreased.

b) Physically this can be interpreted as follows. The secondary-side losses have decreased. Secondary-side losses are incurred during the OFF time of the switch and as such these losses are furnished by the energy discharge from the primary inductance. This means that the primary inductance need not store that much extra energy, and thus, its value can be reduced. In PIXIs designs, Z is always set as an input as shown in Figure 1.



	A	B	C	D	E	F
1	ACDC_PeakSwitch_031006; Rev.1.1; Copyright Power Integrations 2006	INPUT	INFO	OUTPUT	UNIT	ACDC_PeakSwitch_031006_Rev1-1.xls; PeakSwitch Continuous/Discontinuous Flyback Transformer Design Spreadsheet
2	ENTER APPLICATION VARIABLES					Customer
3	VACMIN	85			Volts	Minimum AC Input Voltage
4	VACMAX	265			Volts	Maximum AC Input Voltage
5	fL	50			Hertz	AC Mains Frequency
6	Nominal Output Voltage (VO)	24.00			Volts	Nominal Output Voltage (at continuous power)
7	Maximum Output Current (IO)	0.75			Amps	Power Supply Output Current (corresponding to peak power)
8	Minimum Output Voltage at Peak Load			24.00	Volts	Minimum Output Voltage at Peak Power (Assuming output droop during peak load)
9	Continuous Power	6.00		6.00	Watts	Continuous Output Power
10	Peak Power			18.00	Watts	Peak Output Power
11	n	0.70				Efficiency Estimate at output terminals and at peak load. Enter 0.7 if no better data available
12	Z			0.60		Loss Allocation Factor (Z = Secondary side losses / Total losses)
13	tC Estimate	3.00			mSeconds	Bridge Rectifier Conduction Time Estimate
14	CIN	47.00		47	uFarads	Input Capacitance

Figure 1: Screen capture from the PeakSwitch design spreadsheet showing where the Z factor can be entered.

Question 2

Indicate in the above design which of the highlighted losses are primary (P) or secondary-side (S) losses.

Show the Answer

Answer 2

A) Input Stage - The significant loss here occurs due to the input current that flows while the rectifier diodes are conducting. As the energy loss associated is not stored in the inductor this is a primary-side loss

B) Primary-Side Clamp - The equivalent circuit of the primary-side clamp is the same as that of a secondary winding. The clamp circuit dissipates power during the OFF time of the switch. As such, the energy associated with this loss must be stored in the inductor and thus, it is a secondary-side loss

C) Transformer Node Drain capacitance - Drain-node capacitance loss occurs primarily during turn on event wherein power is being processed by the switch and energy is being stored in the primary inductance. Thus it is a primary-side loss.

D) Transformer Losses :

a. Transformer core loss - Core losses are independent of ON or OFF time. The energy associated with this loss must be stored within the primary inductance. This is therefore a secondary-side loss

b. Transformer Winding loss - Losses associated with the primary winding portion are primary-side losses and losses associated with the secondary-side winding are secondary-side losses.

E) PeakSwitch Losses :

a. PeakSwitch Switching Loss - This is a complicated loss to assign to either primary or secondary-side. The turn-on losses are primary-side losses but the turn-off losses are secondary-side losses. Since turn-off losses are usually more dominant, a conservative approach would be to assign these losses to the secondary-side

b. PeakSwitch Conduction Loss - These losses occur during the ON time of the switch. Thus they are primary-side losses.

F) Output Rectifier and Snubber - Rectifier losses occur during OFF time, while the diode is conducting, and cause the diode snubber capacitor to charge. However actual losses within the snubber occur when the MOSFET turns on, discharging the snubber capacitor. Since the energy in the capacitor was processed during the OFF time though, they are still considered secondary-side losses.
G) Bias Winding Power - The Bias winding looks like a secondary winding, thus it conducts during the OFF time. It is a secondary-side loss.
H) Current Sense - This loss takes place on the secondary side, and is a secondary-side loss.

Question 3

For the following supplies would you expect the Z factor to be less than 0.5 (Primary dominated losses), equal to 0.5 (Balanced losses) or greater than 0.5 (Secondary dominated losses)? In what ways would you verify the Z factor in the above design?

Power Supply Application	P, B or S
3 W Cell Phone Charger	
25 W Set-top box supply	
DC input standby power supply	
32 W (81 W peak) inkjet printer supply	

Show the Answer

Answer 3

Part 1

3 W Cell Phone Charger (Secondary Dominated)
The secondary-side CC (Constant Current) sense circuit is usually associated with significant losses (secondary dominated losses). This extra energy must be stored within the primary inductance. The estimated Z factor is 0.7.
25 W Set-Top Box Supply (Balanced) Here, as the output power has increased, the input stage will no longer use a fusible resistor and the EMI filter inductors will be replaced with a common-mode choke, both of which will reduce the input stage losses. No secondary CC circuits are required so primary and secondary-side losses should roughly balance out. The estimated Z factor is 0.5.
DC Input Standby Power Supply (Secondary Dominated) The secondary-side losses would slightly dominate in this power supply arrangement because there is no input stage - no rectifier or filter. (In the presence of a rectifier and filter the losses would roughly balance out.)
32 W (81 W Peak) Inkjet Printer Supply (Secondary Dominated) Usually inkjet printers have a need for high peak-to-average power. Often the output components and transformer-winding wire size are rated for the average power and average thermal rise. However, the instantaneous loss during the peak load condition is high. In addition, such designs may have large primary-to-secondary turns ratios (large VOR). This usually translates into higher secondary RMS currents, which also lead to higher secondary-side losses. The estimated Z factor is 0.6.

Part 2

Verification of Z factor for the design shown

The prototype shown was run at 88 VAC input and at 65 W output (27.74 V, 2.34 A). Total input power was measured as 88.5 W, giving an overall efficiency of 73.3%. That means that the total losses in the power supply, P_{LOSS}, were 23.59 W.
The following are the prominent areas where losses can be categorized as primary-side losses. All other losses will therefore be secondary-side losses.
1) MOSFET Conduction Losses, P_{COND}
2) MOSFET Switching Losses (Portion of Turn -Off Losses), P_{SW_PRI}
3) EMI Filter Losses, P_{EMI}
4) Diode Bridge Conduction Losses, P_{DIODE}
5) Primary Winding Copper Losses, P_{COPPER}
6) Input Bulk Capacitor ESR Losses, P_{ESR}

We need the following parameters to calculate each of the abovementioned losses. Values in parentheses were the measured values for each of the parameters.
(i) Primary RMS Current, I_{SW_RMS} (1.31 A)
(ii) AC Input RMS Current I_{AC_RMS} (1.39 A)
(iii) Bulk Capacitor RMS current I_{CAP_RMS} (1.107 A)
(iv) Average Diode Current, I_{D_AVG} (0.42 A)
(v) MOSFET RDSON, RDS_{ON} (2.6 Ω)
(vi) Switching Frequency, F_{SW} (299 kHz)
(vii) Common Mode Inductor Wire Resistance, R_{CM} (0.6 Ω)
(viii) Transformer Primary Winding Resistance, R_{PWDG} (0.5 Ω)
(ix) Bulk capacitor ESR, R_{ESR} (0.7 Ω)
(x) MOSFET Switching Transition Time, ΔT(48 ns)
(xi) MOSFET Switching Voltage, V_{SW} (269 V)
(xii) MOSFET Switching Current, I_{SW} (2.42 A)
1) MOSFET Conduction Losses, P_{COND}

$$P_{COND} = I_{SW\_RMS}^{2} \cdot RDS_{ON}$$

$$P_{COND} = 1.31^{2} \cdot 2.6$$

$$P_{COND} = 3.406\,W$$

2) MOSFET Switching Losses (Portion of Turn-Off losses), P_{SW_PRI} The MOSFET switching losses are difficult to allocate as primary-side or secondary-side losses. They affect both sides of the transformer and yet they are significant loss elements. We will therefore allocate half the losses to the primary side and the other half to the secondary side.

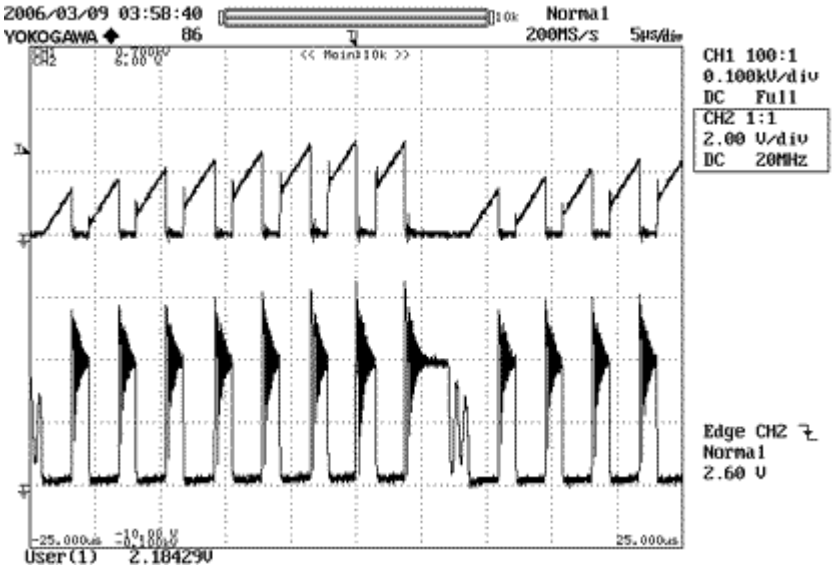


Figure 2. Waveform shows Drain current (Top) and Drain Voltage (Bottom).

Additionally, it can be observed from Figure 2 that this power supply skips 1 cycle out of every 9 switching cycles to maintain output regulation. We will factor this into the total switching losses

$$P_{SW} = \frac{1}{2} \cdot \left(\frac{1}{2} \cdot V_{SW} \cdot I_{SW} \cdot \Delta T \cdot F_{SW} \cdot \frac{8}{9} \right)$$

$$P_{SW\_PRI} = \frac{1}{2} \cdot \left(\frac{1}{2} \cdot 269 \cdot 2.42 \cdot 48 \cdot 10^{-9} \cdot 299 \cdot 10^{3} \cdot \frac{8}{9} \right)$$

$$P_{SW\_PRI} = 2.07\,W$$

3) EMI Filter Losses, P_{EMI} Since there are 2 chambers for a common-mode inductor this loss will be incurred two times.

$$P_{EMI} = 2 \cdot I_{AC\_RMS}^{2} \cdot R_{CM}$$
$$P_{EMI} = 2 \cdot 1.39^{2} \cdot 0.6$$
$$P_{EMI} = 2.318\ W$$

4) Diode Bridge Losses, P_{DIODE}

$$P_{DIODE} = 4 \cdot V_{D} \cdot I_{D\_AVG}$$
$$P_{DIODE} = 4 \cdot 0.7 \cdot 0.42$$
$$P_{DIODE} = 1.1704\ W$$

5) Primary Winding Copper Losses, P_{COPPER}

$$P_{COPPER} = I_{RMS}^{2} \cdot R_{PWDG}$$
$$P_{COPPER} = 1.31^{2} \cdot 0.5$$
$$P_{COPPER} = 0.8580\ W$$

6) Bulk Capacitor ESR Losses, P_{ESR}

$$P_{ESR} = I_{CAP\_RMS}^{2} \cdot R_{ESR}$$
$$P_{ESR} = 1.107^{2} \cdot 0.7$$
$$P_{ESR} = 0.6644\ W$$

The total primary-side losses, P_{LOSS_PRI} are therefore
$P_{LOSS\_PRI} = P_{COND} + P_{SW\_PRI} + P_{EMI} + P_{DIODE} + P_{COPPER} + P_{ESR}$
P_{LOSS_PRI} = 10.4868 W
Thus the total secondary-side losses P_{LOSS_SEC} can be written as $P_{LOSS\_SEC} = P_{LOSS} - P_{LOSS\_PRI}$
P_{LOSS_SEC} = 13.1 W
By definition of the Z factor

$$Z = \frac{P_{LOSS\_SEC}}{P_{LOSS}}$$
$$Z = 0.5557$$

Puzzler 12

Test your power supply design knowledge as it pertains to printed circuit board layout by trying your hand at answering the three questions below, then check your answers to see how well you did.

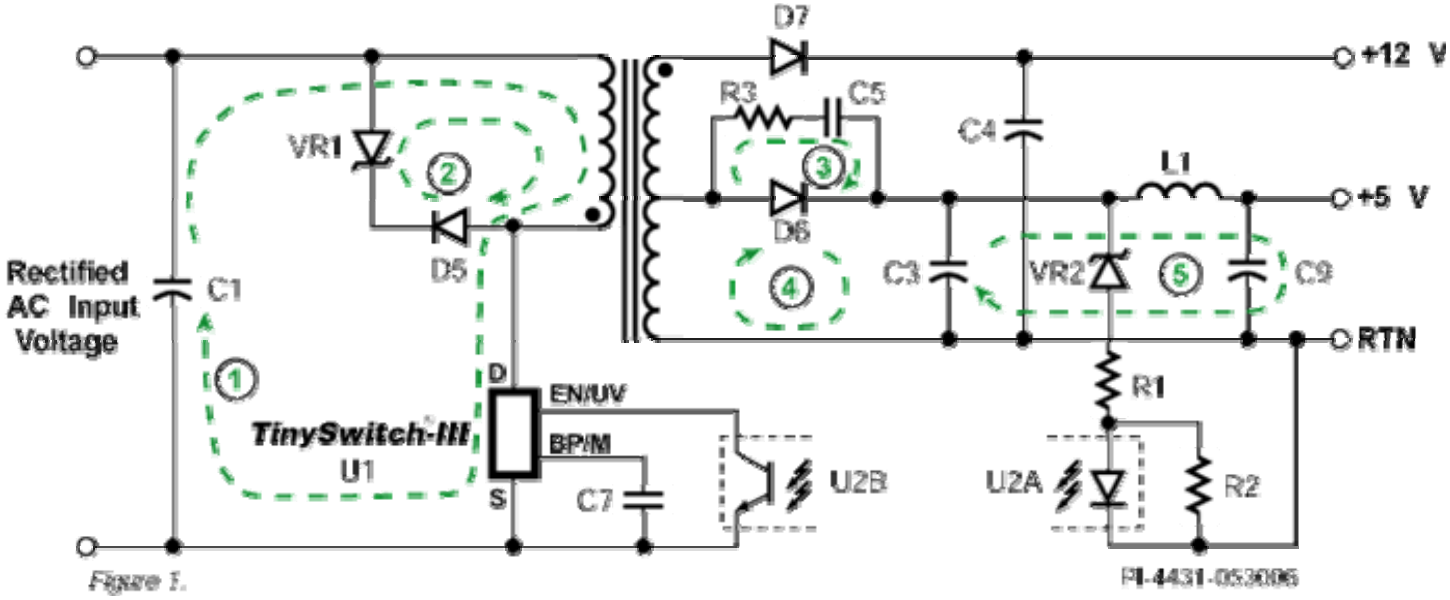


Figure 1.

Question 1

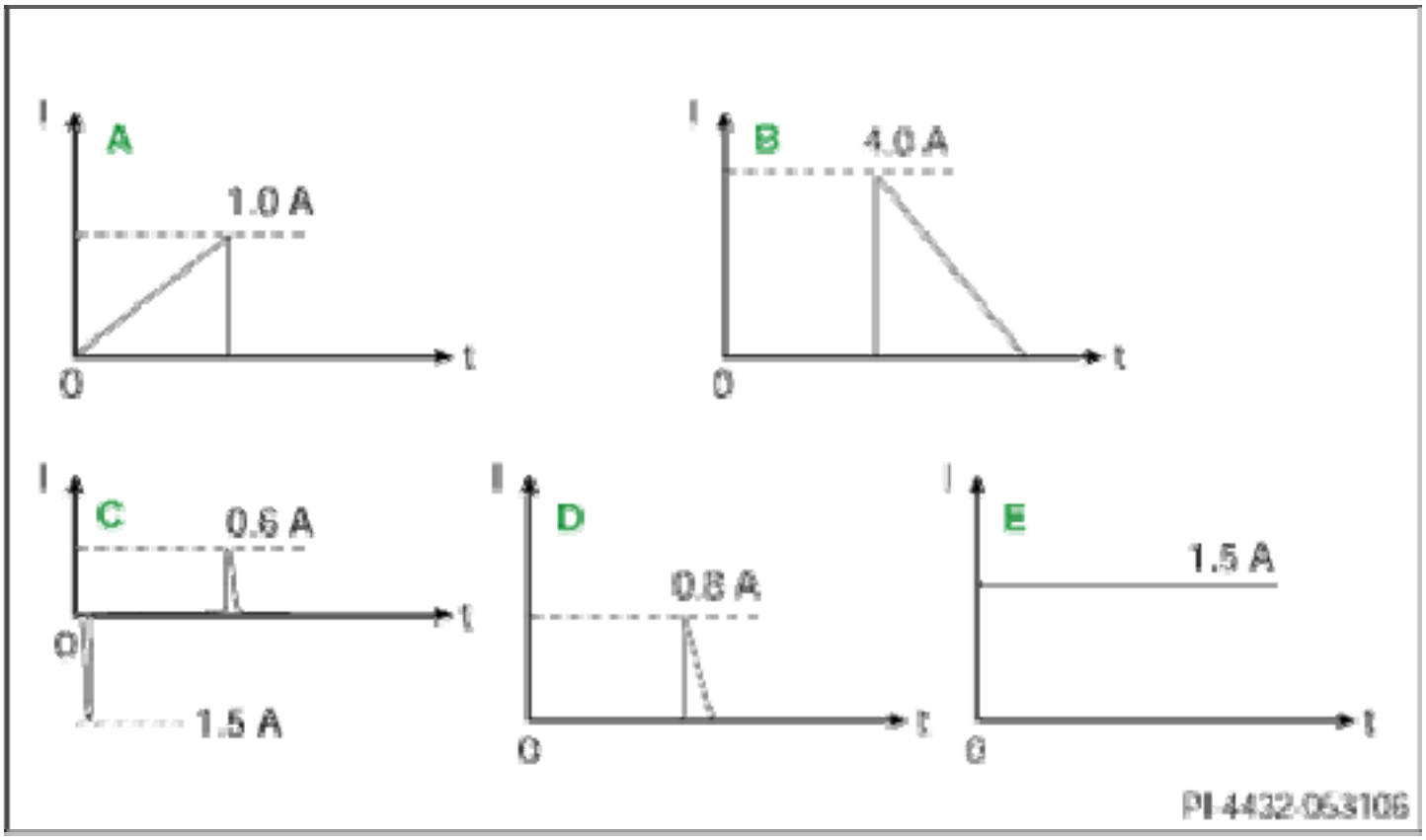


Figure 2.

Match each of the current waveforms shown in Figure 2 to the five current loops shown in Figure 1.
The X-axis represents time, where t=0 is the start of a switching cycle (U1 internal MOSFET turns on). The Y-axis represents current, with the peak current values indicated on each waveform.

A. _____ B. _____ C. _____ D. _____ E. _____

Show the Answer

Answer 1

a. This waveform is characterized by a steady rise of current and this rise continues for the duration of the ON time. This characteristic linear ramp is representative of the Drain current waveform and can be matched to the current flowing through loop 1.

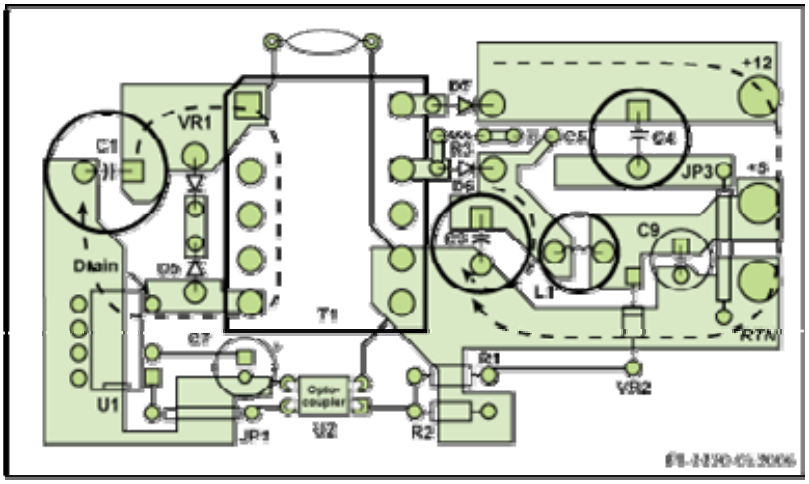
b. This waveform is characterized by a steady fall of current from approximately the end of ON time. This is a characteristic linear ramp down of the secondary diode current and can be matched to the current flowing through loop 4.

c. This waveform has two distinct characteristics - at turn on, a negative current, and at turn off - a positive current spike. The secondary winding voltage has a similar characteristic, negative while the MOSFET is on and positive when the switch is off with the negative voltage being larger than the positive voltage. This cannot be the current through the output diode because the magnitude and duration are too short so it suggests that the current must be flowing through loop 3.

d. This waveform also occurs at the MOSFET turn off transition. At this point the leakage and magnetizing current first charges drain node parasitic capacitances (associated with the MOSFET and transformer). Once the drain voltage exceeds the clamp voltage plus input voltage diode D5 will conduct. As some of the leakage energy has already been reset charging the drain node the actual peak current into the clamp is lower than the peak drain current at turn off. This suggests that it must be flowing through loop 2

e. This DC current is characteristic of the output/load current that flows through loop 5. Capacitor C3 filters the secondary switching current so that only DC currents appear in loop 5.

Question 2



Layout is a crucial step in addressing EMI, specifically making sure loop areas are as small as possible. Figure 1 shows five different loops in a typical Flyback power supply. Arrange these loops according to which loop area is most critical to shrink.

1st _____ 2nd _____ 3rd _____ 4th _____ 5th _____

Show the Answer

Answer 2

First a caveat - These loops have been prioritized with the assumption that the switching device uses a MOSFET with high switching speed (and not a bipolar which typically have lower switching speeds).

There are 4 aspects that decide how critical a loop area is to shrink and thereby minimize radiated noise. These 4 aspects are

1. The absolute magnitude of the switched current
2. The rate of change of the switching current (di/dt)
3. The absolute magnitude of the switching voltage
4. The rate of change of switching voltage (dv/dt)

1. Loop 1

This loop carries the primary switching current. High di/dt currents will create a voltage drop across the impendence of this loop (including the ESR of the input capacitor) and be a source of differential mode EMI. In addition the drain node itself has a high voltage swing together with a high dv/dt and by minimizing the area of this node, the electrostatic coupling and therefore common mode EMI are reduced. Although the absolute magnitude of currents in this loop are smaller than those in loop 4, typically the di/dt is higher and together with the high dv/dt makes this loop the most critical.

2. Loop 4

This loop carries the highest magnitude of switching currents and thus is one of the most powerful radiating antennas in the power supply, as such this loop area must be kept to a minimum. This loop also impacts the leakage inductance losses and therefore primary clamp losses. By minimizing the loop length the trace leakage inductance that is reflected through the transformer (via the turns ratio squared) to the primary is also minimized. Although loop 1 has been designated as most critical this loop is a very close second. Thankfully however, in most power supplies both these loops can be shrunk independently of one another.

3. Loop 2

This loop connects to the primary side clamp circuit. Fast current transients flow within the loop and this area should be minimized. The clamp often causes high voltage, high frequency ringing. Minimizing the loop reduces the coupling of this noise that appears in both conducted and radiated common mode EMI.

4. Loop 3

The primary objective of this loop is to provide a localized pullout current path for the reverse recovery (snap off) current from the secondary diode. The di/dt in this loop is not as high as in loops 1 2 and 3. Furthermore, the peak

currents are usually not comparable to the secondary peak currents. However, this loop can be critical for controlling high frequency radiated EMI and should also have a small loop area.

5. Loop 5

Capacitor C3 filters the secondary switching current so that only low frequency DC current appear in loop 5. Since the switching component of current in this loop is negligible, this loop area is not very critical.

Question 3

Figure 3 shows a partial layout for the two output power supply shown in Figure 1. Can you spot five areas where the layout could be improved? While you are not permitted to add or subtract components, you may reposition them. Black dashed lines indicate the important primary and secondary side loops.

Show the Answer

Answer 3

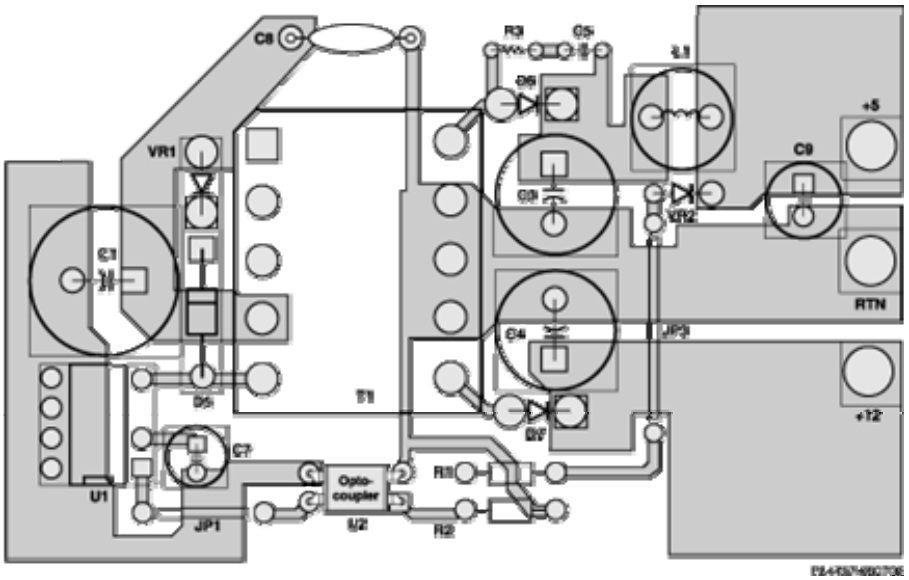


Figure 4: Improved layout for partial circuit shown in Figure 3.

1. Capacitor C1 can be placed physically closer to the switching MOSFET (U1). This facilitates shorter leads to the connecting components thereby reducing trace inductance.
2. The loop area connecting capacitor C1, transformer T1 and switching MOSFET U1 can be minimized as shown in figure 4 above. This is made possible by using pin 4 of the transformer to connect to the positive DC bus, (positive terminal of C1) rather than pin 1, which was used in the original layout.
3. Capacitor C7, which is the bypass capacitor needs to be placed as close as possible to the integrated controller and MOSFET (U1).
4. Drain connection trace width reduced. This section of the track carries high voltage switching signals (high dv/dt). Such signals can capacitively couple to earth ground and cause common mode EMI. A wide trace (larger surface area) would present higher coupling capacitance to earth ground and generate more common mode EMI. Figure 1 shows reduced copper area between transformer and the Drain node. This is also the reason why the connection from transformer T1 to diodes D6 and D7 should not be connected by excessively wide copper traces.
5. Components D7 and C4 are repositioned and the secondary ground has been moved such that the loop area for both the outputs are now minimal. In general for multi output designs it is a good practice to layout the ground trace in the middle of the transformer. This minimizes loop area and improves radiated EMI performance. If you have more than 2 outputs, prioritize the outputs according to highest currents and position the highest current output to have the smallest loop area.
6. Post filter capacitor C9 has been moved physically closer to the output terminals. This minimizes the inductance to the output terminals and reduces output ripple and noise.
7. Y capacitor connection tracks are thick in Figure 3. This is better for high frequency EMI performance. Thicker tracks provide lesser impedance (resistive as well as inductive) at higher frequencies.

Puzzler 13

Test your knowledge of designing printed circuit board layouts for power supplies by answering the three questions below.

The circuit below shows a three output VoIP telephone power supply using a *DPA-Switch* power conversion IC. The low-cost discrete PoE interface circuit identifies the supply as Class 3 per IEEE802.3af. Class 3 limits the maximum power drawn from the network cable to 12.95 W.

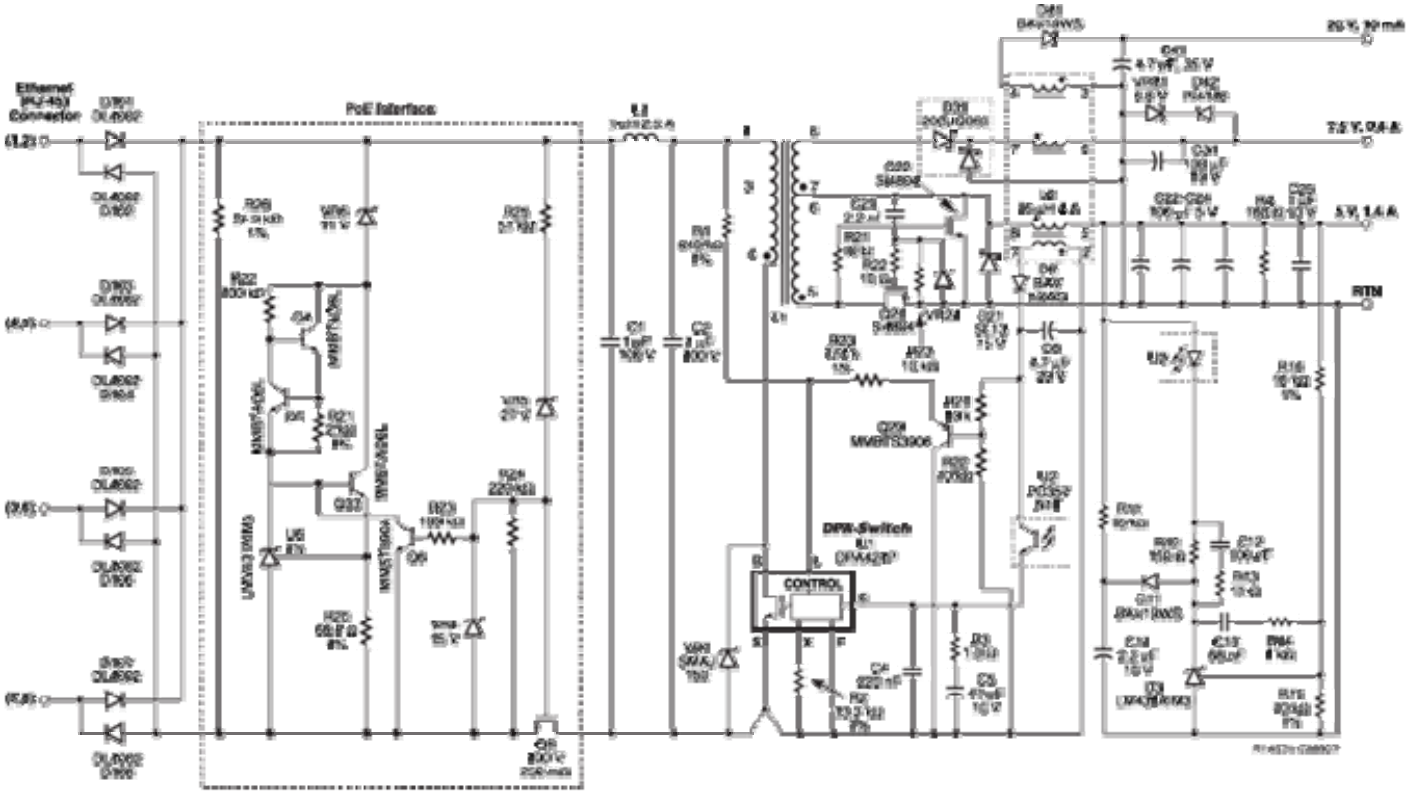


Figure 1. Picture of forward converter with synchronous rectifier and DAK-06 PoE ext.

Question 1

As new features are added to PoE powered products, for example a color display or camera to a VoIP phone, the power requirements often rise. Why is it desirable to increase efficiency in the PoE power supply as load requirements rise?

Show the Answer

Answer 1

With a fixed input power limit, increases in efficiency directly increase the amount of power that can be delivered to the output. For example at 75% efficiency the available output power is 9.7 W but at 85% efficiency that rises to 11 W.

Question 2

Part 1

Synchronous rectification is employed to boost the efficiency of the output stage. For a single output 3.3 V, 3 A forward converter what would you estimate the increase in output power to be by changing from diode rectification to synchronous rectification (Q21, Q22) as shown in Figure 1? Assume the following:

1、 Converter operating on duty cycle of 50%
2、 Schottky diode VF of 0.4 V
3、 MOSFET RDS(ON) of 30 mW and operating duty cycle of 50%.

Part 2

The DPA-Switch (U1) used in this design has a programmable current limit. By changing the value of R2 the current limit can be programmed from 100% to 30% of the internal maximum. What single component change does this feature allow the designer to make for higher efficiency without changing anything else in the design? Is there a limit to this approach?

Show the Answer

Answer 2

Part 1

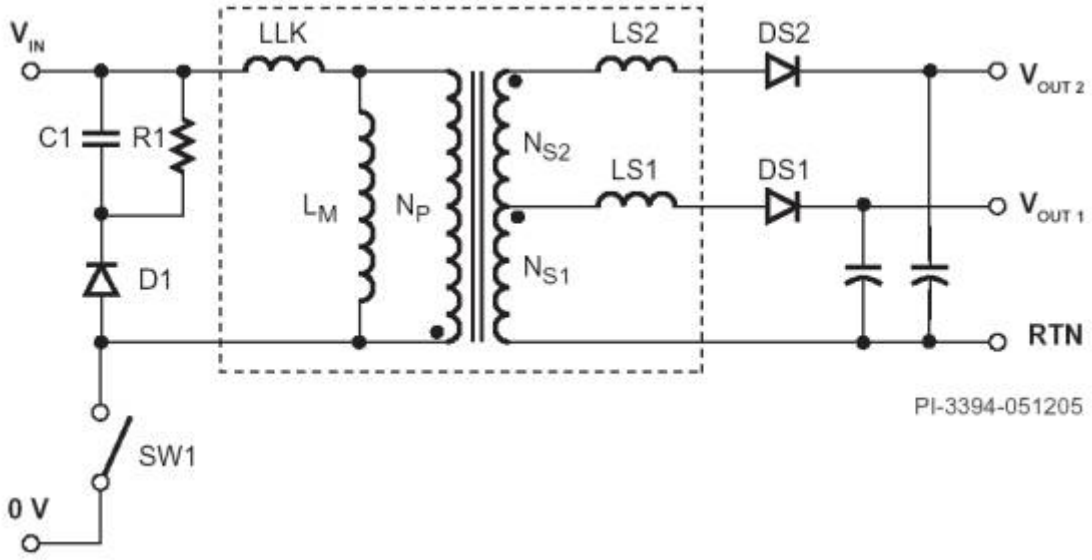
1. Diode Rectification Case

The average current in the output diodes is equal to the output current multiplied by the duty cycle.

$$P_{D(ON)} = I_{OUT} \times V_F \times D$$
$$= 3\,A \times 0.4\,V \times 0.5$$
$$= 0.6\,W$$
$$P_{D(OFF)} = I_{OUT} \times V_F \times (1-D)$$
$$= 3\,A \times 0.4\,V \times 0.5$$
$$= 0.6\,W$$
$$P_{D(TOTAL)} = P_{D(ON)} + P_{D(OFF)}$$
$$= 1.2\,W$$

2. Schottky Rectification Case

As the voltage drops across the MOSFETs are not constant we need to calculate the RMS current through both devices.



$$I_{RMS(Q2)} = I_{OUT} \times \sqrt{1-D}$$
$$= 3 \times \sqrt{1-0.5}$$
$$= 2.12A$$

$$I_{RMS(Q1)} = I_{OUT} \times \sqrt{D}$$
$$= 3 \times \sqrt{0.5}$$
$$= 2.12A$$

So we see that the 50% duty cycle will result in identical dissipation in both MOSFETs (for identical MOSFETs).

$$P_{Q1} = P_{Q2} = I_{RMS}^2 \times R_{DS(ON)}$$
$$= 2.12^2 \times 30\,m\Omega$$
$$= 0.134\,W$$

$$P_{TOTAL} = P_{Q1} + P_{Q2}$$
$$= 0.134\,W + 0.134\,W$$
$$= 0.268\,W$$

Total dissipation in the MOSFETs is 0.269 W.

3. Increase in Output Power

Increase in output power is the difference in losses between the two rectification schemes:

1.2 W - 0.269 W = **0.93 W**

In practice the real world improvement is somewhat lower than this. For example the MOSFET drive losses have been excluded and with passive drive the freewheeling MOSFET is only driven for part of the off time (up until the transformer is reset).

Part 2

The programmable current limit allows the selection of a larger DPA-Switch device with a lower $R_{DS(ON)}$ MOSFET. The lower $R_{DS(ON)}$ lowers conduction losses and improves efficiency. The programmable current limit allows the current limit of the larger device to be programmed to be the same as the original, smaller device. This avoids the need to change the transformer or the rest of the circuit to operate at a higher peak primary current.

There is a limit to this approach because as a larger device is selected for lower $R_{DS(ON)}$, the MOSFET capacitances also increase, causing an increase in switching losses. Therefore for a given design, operating frequency and input voltage there is an optimum device size that minimizes switching and conduction losses. Typically this is one device size larger (half the value of $R_{DS(ON)}$).

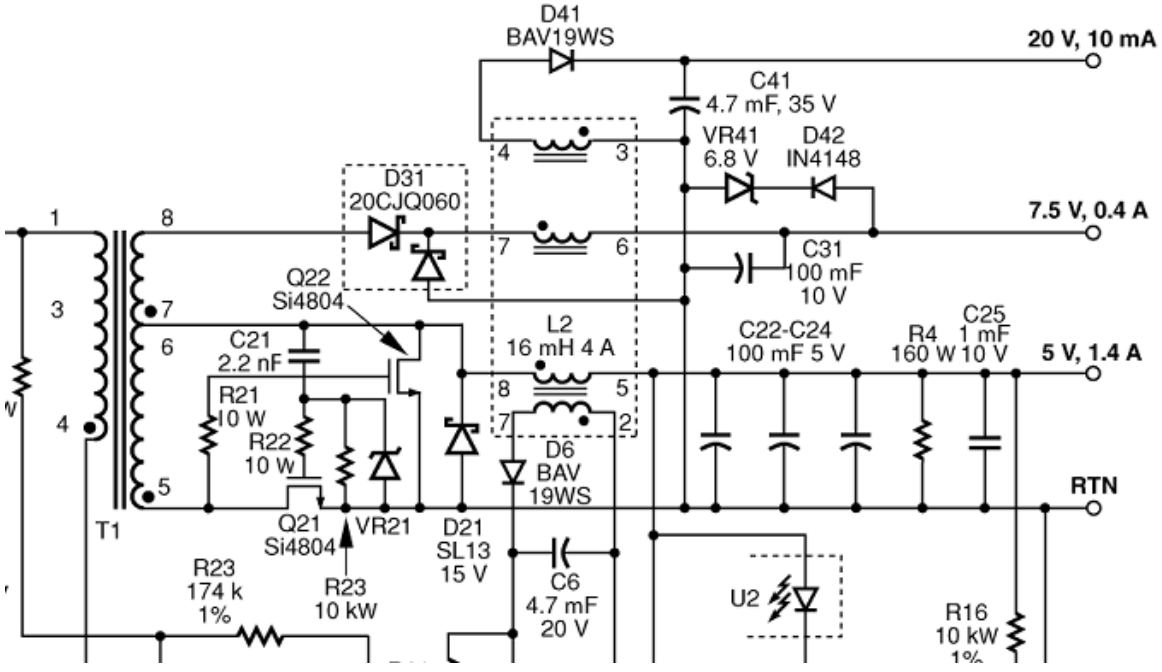
Question 3

Again, referring to Figure 1, what is the role of C21 when connected in series with Q21 in the synchronous rectification circuit?

Show the Answer

Answer 3

1. Capacitor C21 is added to prevent an abnormal condition that occurs during brown out or power down.



If C21 is omitted during normal operation the converter will operate normally, the positive voltage that appears across the secondary winding during the on-time of the primary switch will turn on Q21.
However once the primary stops switching the current through L2 will ramp to zero delivering energy into the output capacitors. If the output capacitors are close to the output voltage then at the point the L2 current falls to zero a positive voltage appears at the gate of Q21, turning it on and allowing the current to ramp in the opposite directly through L2. The current loop formed is from the output capacitors (C22-C24), L2, the secondary winding of T1 and Q21 back to the output capacitors.
The current ramp eventually causes the transformer core (T1) to saturate at which point the gate drive for Q21 is removed and it starts to turn off. The energy in L1 and T1 cause an inductive voltage spike to appear at the gate of Q22, turning it on and reducing the gate drive of Q21.
The magnitude of the voltage spike seen by Q22 is typically much greater than its maximum rating causing device failure.
By adding C21, when switching stops, the DC voltage that appears at the gate of Q21 when the L2 current reaches zero is blocked, preventing Q21 turning one and therefore preventing the conditions that can damage Q22.
During normal operation C21 acts as a charge pump, providing sufficient charge to turn on Q21 as the secondary winding voltage swings positive, with the maximum gate voltage clamped by VR21. As the secondary winding swings negative, C21 is discharged (reset) via VR21, ready to turn on Q21 on the next switching cycle.

Puzzler 14

Test your power supply printed circuit board layout design skills by trying your hand at answering the three questions below. To enter for a chance to win a new Apple iPod nano, click on the iPod image following Question 3.
The feedback circuit shown in Figure 1a was used for a 24 V, 2.5 A design. The design was created using PI Expert. The bode plots shown in Figure 1b represent loop response without using the components RF4 and CF2.

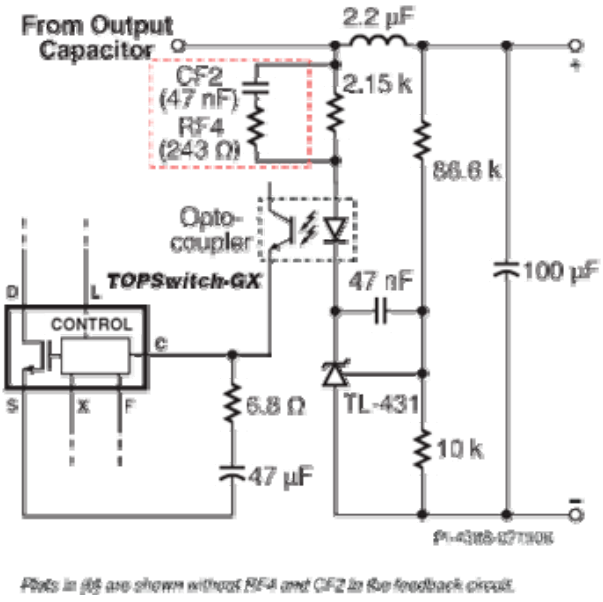


Figure 1a

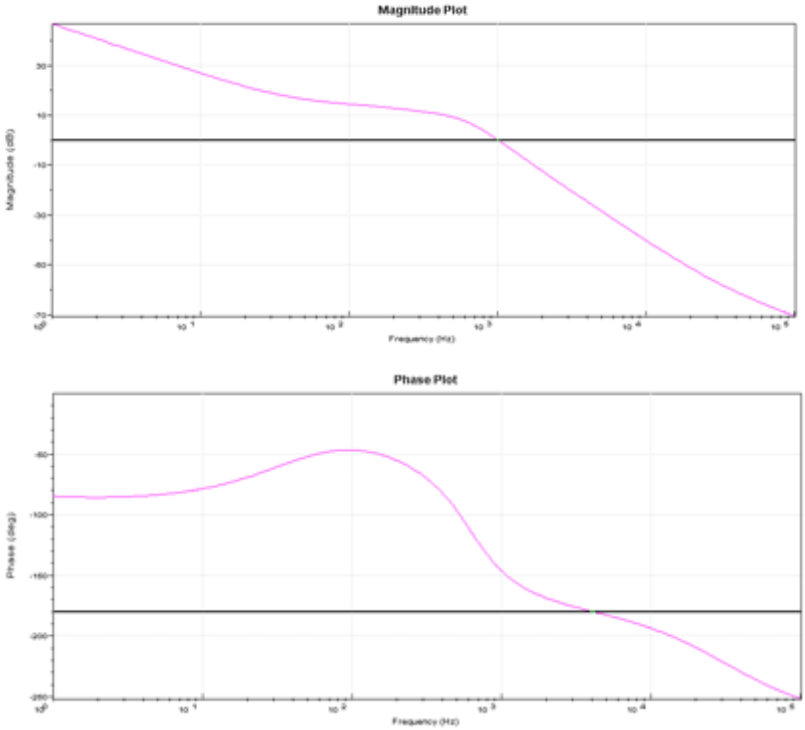


Figure 1b

Plots in (b) are shown without RFPlots in (b) are shown without RF4 and CF2 in the feedback circuit

Question 1

Which statement(s) best describes the primary function of the feedback loop in a switching power supply?

a. Reduces variation in the output voltage due to tolerances of components such as the transformer inductance and output capacitance.
b. Reduces variation in the output voltage due to variations in the input voltage and/or output load.
c. Improves power supply efficiency.
d. All of the above.
e. None of the above.

Show the Answer

Answer 1

The answer is (a) and (b)

The primary objective of the control loop is to stabilize the power supply against variations in component values over production, as well as variations in line voltage and output load.

When an oscillating power supply is stabilized, there is also an added benefit of increased throughput efficiency. Thus the feedback loop also plays a role in improving the efficiency, although this is not its primary objective.

Question 2

a. What is gain margin and phase margin?
b. Figure 1b shows the bode plot of the partial schematic shown in figure 1a. How much gain margin and phase margin does this design have?

Show the Answer

Answer 2

(a) For a control loop to become unstable and oscillate two conditions must simultaneously exist

1. The phase response from input to output will be -180° (assuming 0° phase shift at DC).
2. The loop gain of the system will be 0dB (gain cross over).

Gain margin is the absolute value of the measured loop gain at phase crossover (where the phase has crossed -180°).

Phase margin is the measured phase above-180° at the gain crossover frequency. The value represents the amount the phase would have to reduce by (that is, lag) to meet the criteria for instability.

A well-designed system should have at least 6 dB of gain margin and 45° to 60° of phase margin.

(b) 1 kHz cross over frequency, 33° Phase margin, and 30 dB gain margin.

Question 3

a. A phase boost network was added to the circuit in Figure 1a. What does this network accomplish?
b. What is conditional stability and how does it manifest itself in the operation of the power supply?

Show the Answer

Answer 3

(a) The phase boost network adds a pole-zero pair to the controller transfer function. The component values are chosen in such a manner so that the zero is added at a frequency close to the crossover frequency, and the pole is placed a decade apart, thereby increasing the phase margin of the system.

The PI Expert design tool calculates values for feedback components, provides gain phase plots, and recommends when a phase boost network should be used.

(b) The resultant gain and phase response is shown below. Cross over frequency is 1.1 kHz, the gain margin is 30 dB and phase margin 64°.

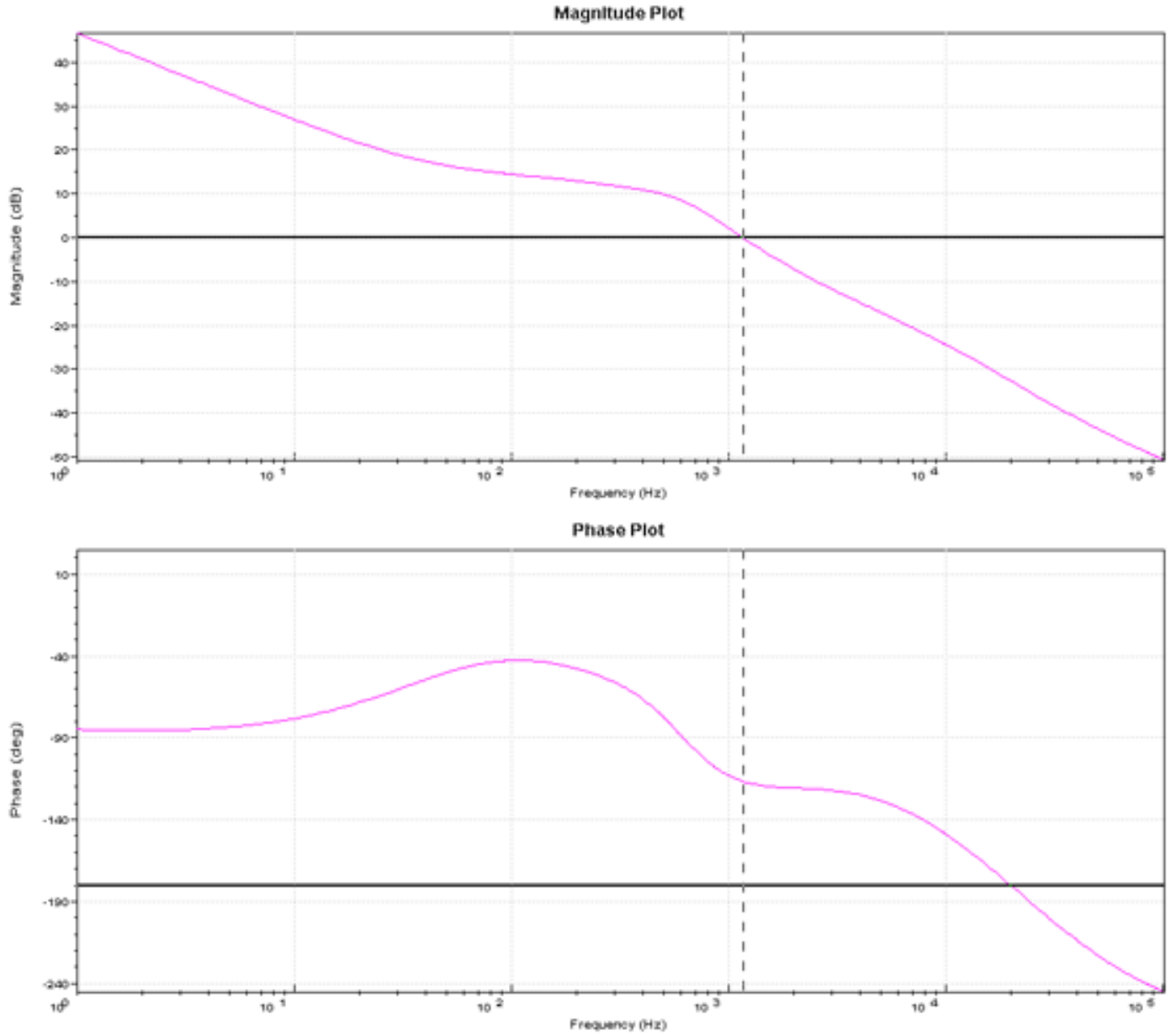


Figure 2

Should the phase margin reduce to zero (phase reaches or exceeds -180°) while the gain is greater than zero, then the loop is considered conditionally stable.

Although theoretically a system with a phase margin of 1° is considered stable, in practice the phase margin in a power supply can vary significantly due to component tolerances and line and load variations.

Conditional stability is therefore not desirable, as in this state these variations can cause the loop gain to reduce, shifting the gain cross over to a lower frequency, where phase margin is inadequate, and causing the power supply to become unstable and oscillate.

This often happens during start-up or other load transients, when the control loop commands maximum or minimum duty cycle.

Puzzler 15

Test your power supply printed circuit board layout design skills by trying your hand at answering the three questions below.

The circuit below shows a 12 V, 1 A power supply using a TinySwitch-III power conversion IC. Capacitors C1 and C2 form the bulk capacitance for this set-up.

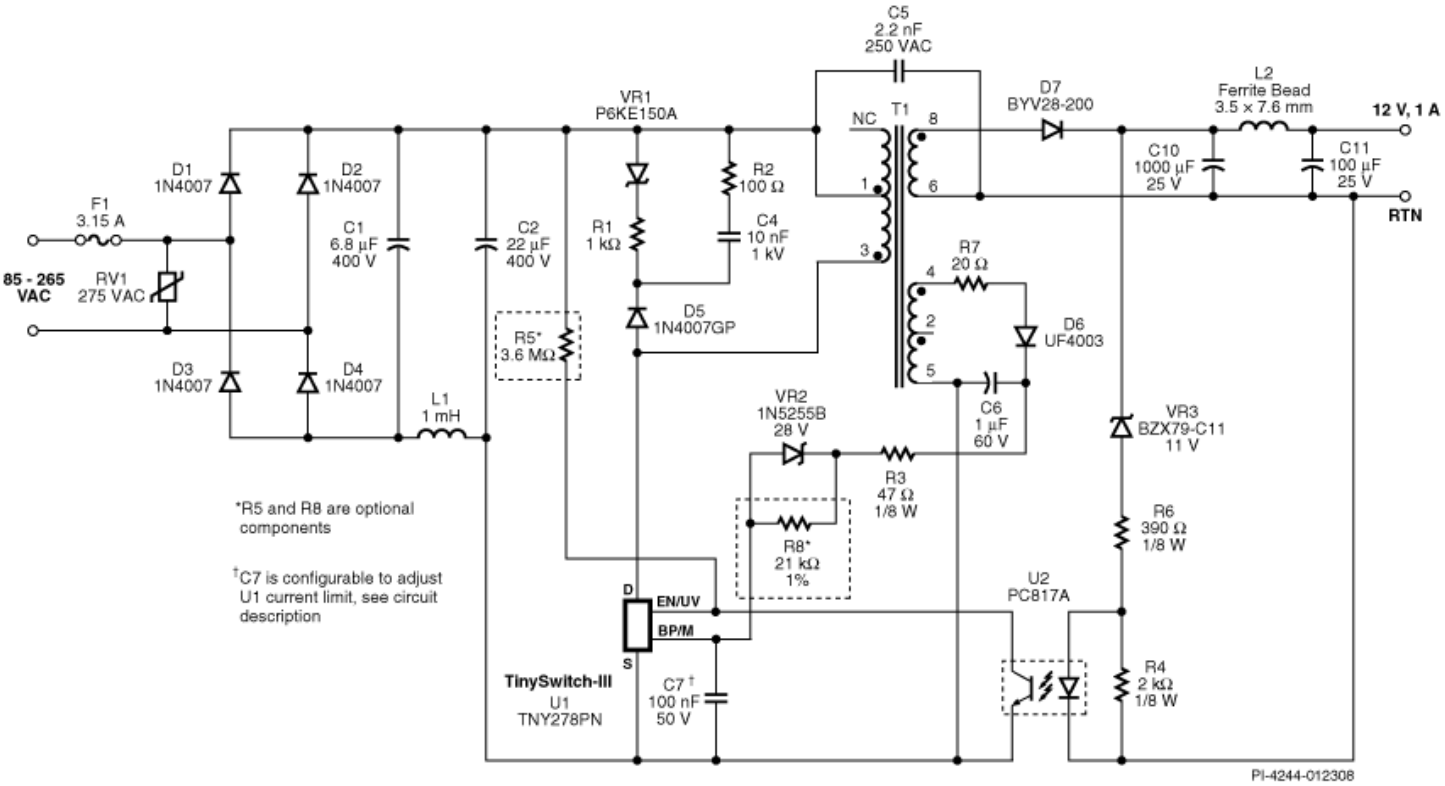


Figure 1. 12 W Universal input flyback power supply

Question 1

What is the relation between the terminal voltage of a capacitor and the energy stored in it?

1. Energy stored in the capacitor is same as the terminal voltage
2. Energy stored is independent of terminal voltage
3. Energy stored is proportional to two times the terminal voltage
4. Energy stored is proportional to square of the terminal voltage

Show the Answer

Answer 1

The answer is d.

Energy stored in a capacitor changes by square of the terminal voltage. A capacitor has 4 times higher energy stored in it if the terminal voltage is doubled.

The relationship between energy stored in a capacitor and its terminal voltage is given by the following equation:

E Energy stored in joule

C Capacitor value in farad

V Capacitor terminal voltage in volt

Question 2

The power supply shown in figure 1 operates over an universal input range (85-265 VAC, 50 Hz/60 Hz) and has a full load efficiency of 75% at 85 VAC. Assuming the supply can operate to a minimum DC voltage of 75 V and there is no hold-up requirement, what is the minimum size of the input DC bus filter capacitor required for every watt of output power delivered?

a. 1.5 µF / W	b. 3.0 µF / W
c. 2.5 µF / W	d. 4.5 µF / W

Show the Answer

Answer 2

C. 2.5 µF / W

Specification of a typical universal input power supply demands satisfactory operation over an input voltage range of 90 to 265 VAC. To ensure trouble free operation during supply voltage sags, which may last from 8 ms to 50 ms, some equipment manufacturers reduce the lower limit to 85 VAC.

The input DC bus capacitor supports the operation of the power supply by storing energy during the peak of the input sinusoid and supplying the stored energy to the converter circuit during interval td. (See figure.2)

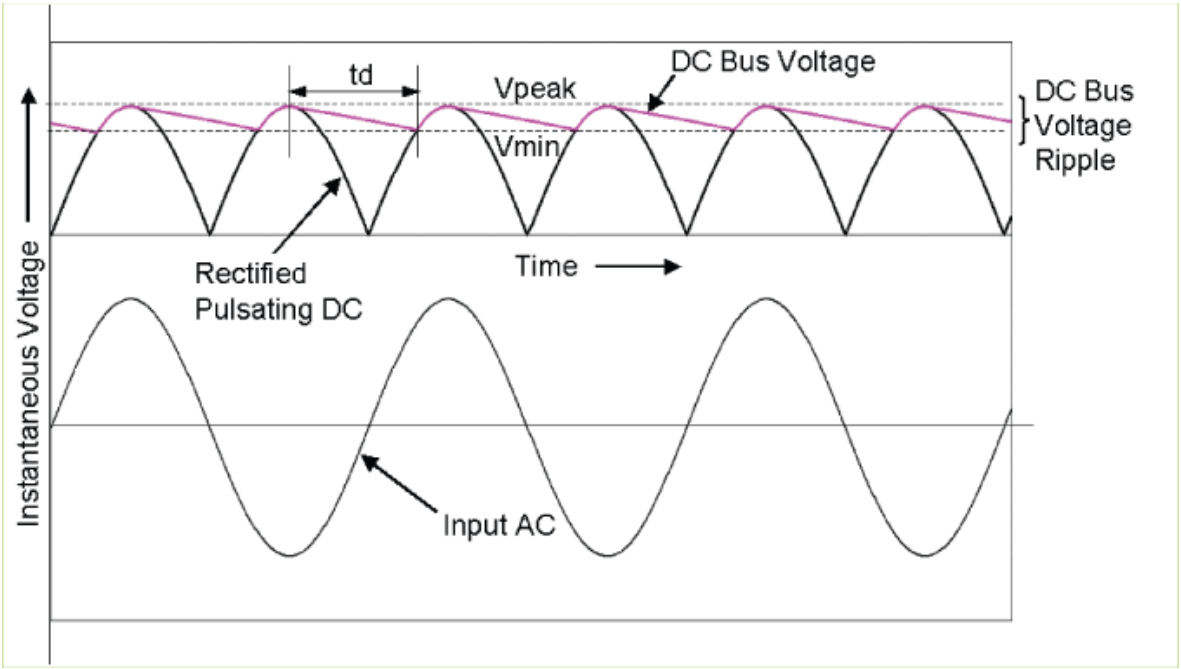


Figure 2. Capacitive filter for full wave rectifier

Calculation of the capacitor value can be made using the equation:

$$C = \frac{2 \times Po \times td}{\eta \times (V_{pk}^{\ 2} - V_{min}^{\ 2})}$$

Po = Converter output power

? = Converter efficiency

td = Capacitor discharge interval

Vpk = Minimum peak voltage seen by the power supply at low line

Vmin = Minimum DC voltage for satisfactory operation

The set of curves in Figure 3 show the result of calculation graphically, for different converter efficiencies and choice of minimum DC bus voltage.

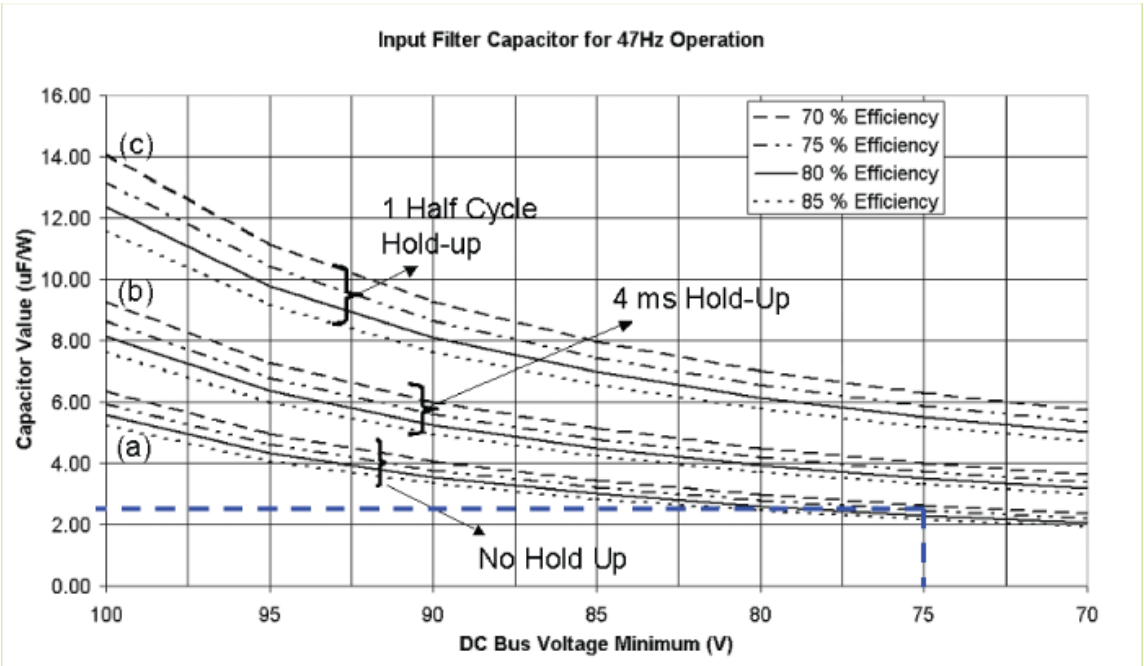


Figure 3. Capacitor selection curves for 47Hz frequency universal input application. (a) No hold up requirement, (b) 4ms hold up requirement and (c) hold up of one half cycle of supply frequency)

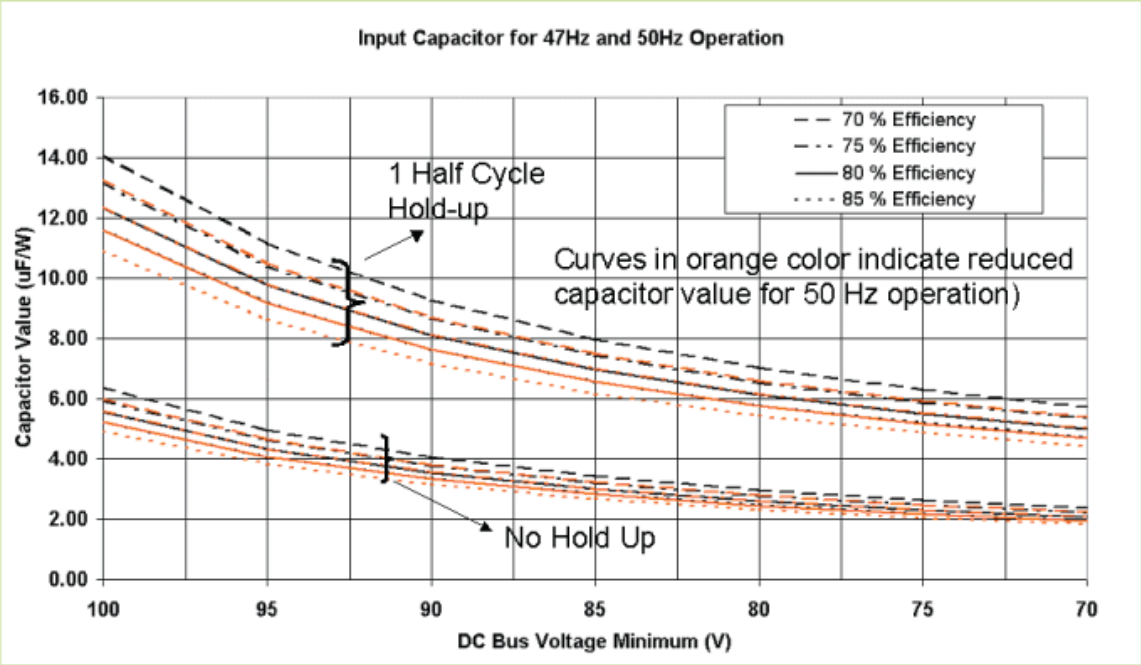


Figure 4. Relative comparison of required capacitor value for 47Hz and 50Hz operation. Notice the slight reduction for a 50Hz only design

A robust design made for worst-case operation would be able to operate satisfactorily for a voltage as low as 85 VAC, line frequency as low as 47 Hz, worst case bulk capacitor, minimum device current limit, minimum primary inductance and minimum switching frequency.

Statistically the probability of these 6 independent variables being at their absolute worst-case values is low. In practice for most applications it is sufficient to design for minimum AC input voltage, typical capacitor values, typical line frequency (50 Hz) minimum current limit, switching frequency (or I^2f for PI products) and primary inductance.

For this example, since the efficiency of the converter is 75% and the converter is designed to operate for a 75 V bus voltage, 2.5 µF / W minimum is required. Higher values would allow operation to a lower voltage or provide hold up time at the expense of larger and higher cost capacitors.

For a power supply with a pi-filter as shown in Figure.1, the capacitor value calculated can be split in two capacitors.

Question 3

Why does removing a maximum duty cycle (maximum on-time) limit in a flyback converter increase energy transfer from the input capacitor as its terminal voltage reduces? Why does this significantly help in applications where data must be stored to non-volatile memory on AC power failure?

Show the Answer

Answer 3

In a flyback converter the energy is first stored in the inductor during the on time of the primary switch and is then delivered to the load during the switch off time. When the AC input fails, the bus voltage falls, reducing the voltage applied across the primary inductance during the switch on time. This reduces the di/dt, requiring a longer on-time to reach peak current.

In a typical converter at some bus voltage the on-time needed to reach current limit is greater than allowed by the maximum duty cycle limit. Once this point is reached the peak inductor current reduces as the bus voltage continues to fall. In effect duty cycle and not peak current now limits the power delivered to the load.

With duty-cycle extension the switch on time is not limited, allowing current limit to be reached regardless of the bus voltage. This maximizes energy transfer from the bulk capacitor to the load. For a given bulk capacitor value this provides a longer hold-up time compared to a power supply with no duty cycle extension.

Most microprocessor-based circuits need power supplies that have adequate hold-up time for multiple reasons:

1. To enable uninterrupted operation during sub cycle supply line disturbances.

2. Microprocessor based applications often need several milliseconds to store critical data to NVRAM or EEPROM memories once a "supply-fail" condition is detected. Output regulation should be maintained to ensure graceful shutdown with no loss of data.

Microprocessor based circuits can reduce power consumption by disabling non-critical loads once input supply failure is detected. For a reduced power level, Flyback converters with on time extension can maintain regulation at the output to a significantly lower DC bus voltage. With the ability to maximize energy transfer to the load the on time extension feature enables the use of lower input capacitor values while still providing adequate holdup time.

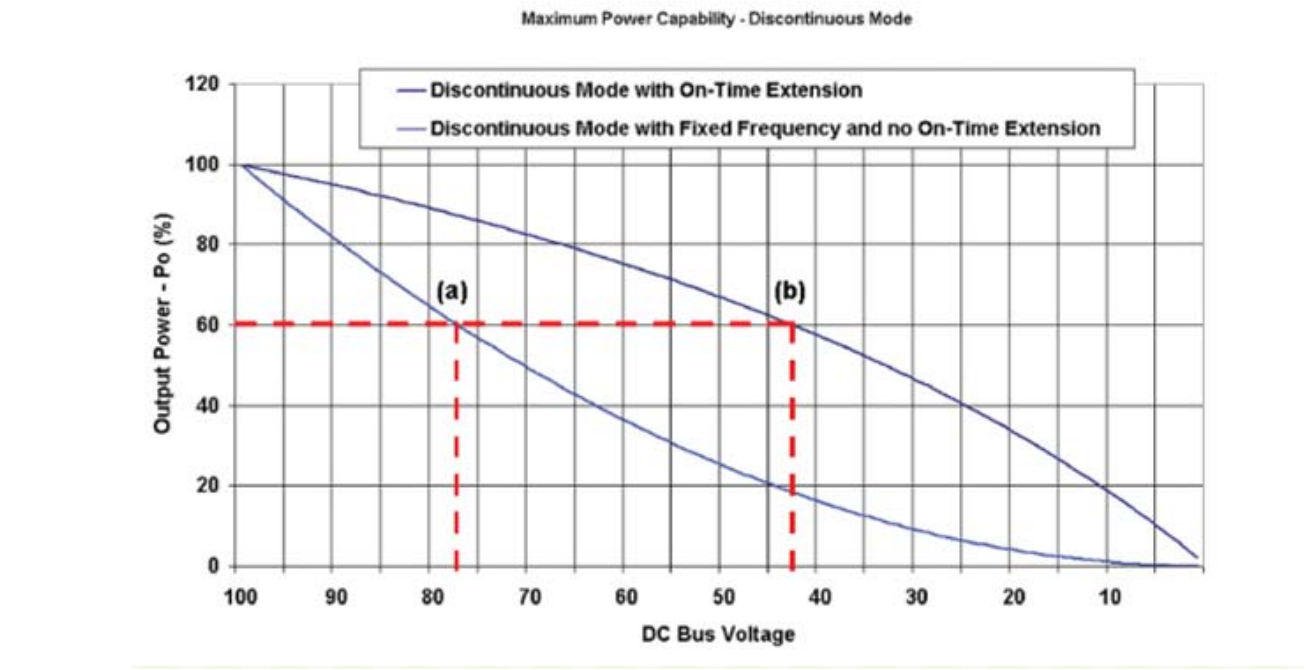


Figure 5. Relation between DC Bus Voltage drop and power delivery capability of Flyback power supplies with and without on time extension. At 60% load regulation is lost at 77 V (a) without on-time extension and 43 V (b) with on-time extension.

Figure. 3 shows that with on time extension a power supply designed to operate with a minimum DC bus voltage of 100 V can deliver up to 60% of its rated load for a DC bus voltage as low as 43 V. A conventional Flyback converter under the same conditions but without on-time extension will fall out of regulation as soon as DC bus voltage drops below 77 V.

This explains why converters with on time extension provide longer hold up time as compared to fixed frequency solutions especially for reduced load levels without any additional changes in the design.

Figure 4 shows an example of improvement in hold-up time of the 12 V, 1 A power supply show in figure 1 operating at full load due to use of on time extension.

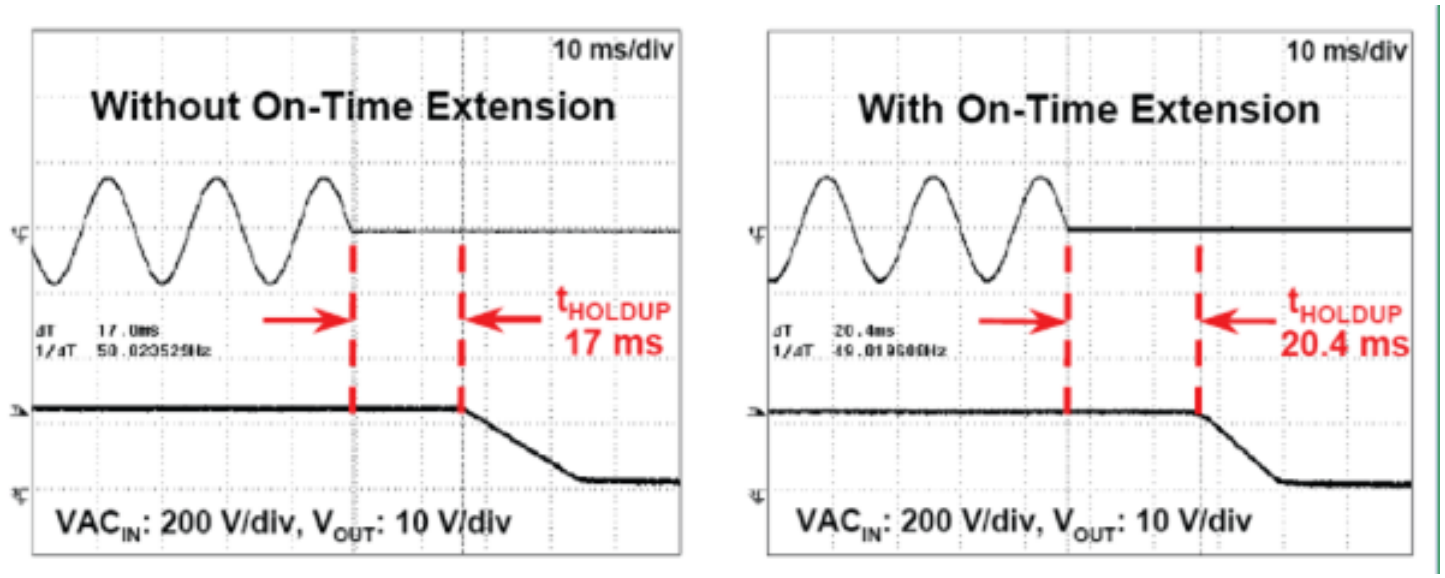


Figure 6. Improvement in hold up time with on time extension